FIG. 1A

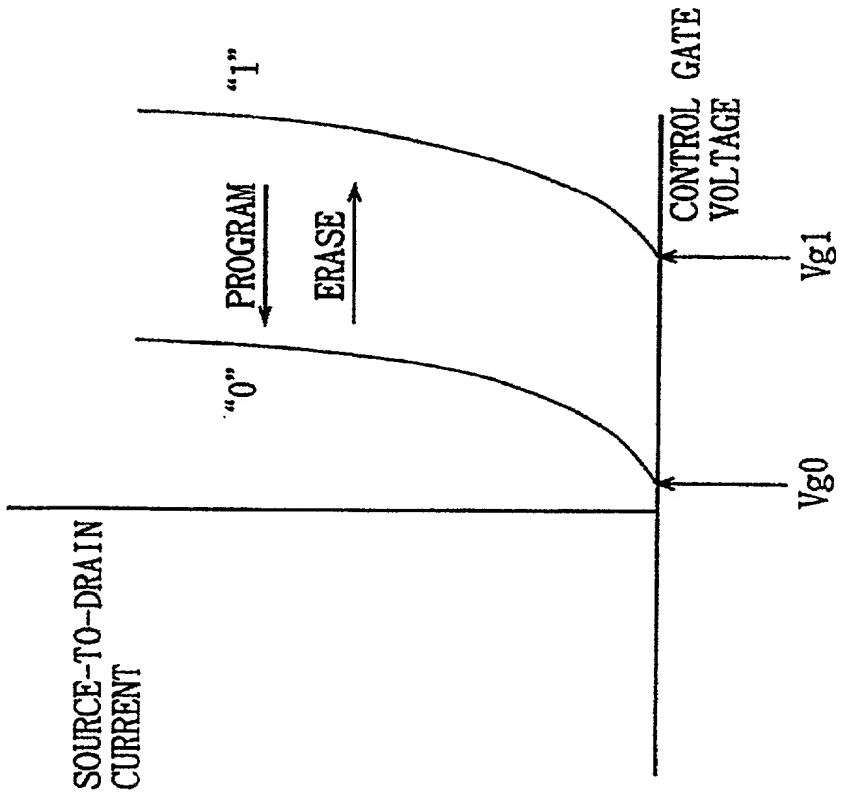

(INVENTION)
SOURCE-TO-DRAIN CURRENT
"0"
"1"
PROGRAM
ERASE
CONTROL GATE VOLTAGE
Vg0
Vg1

FIG. 1B

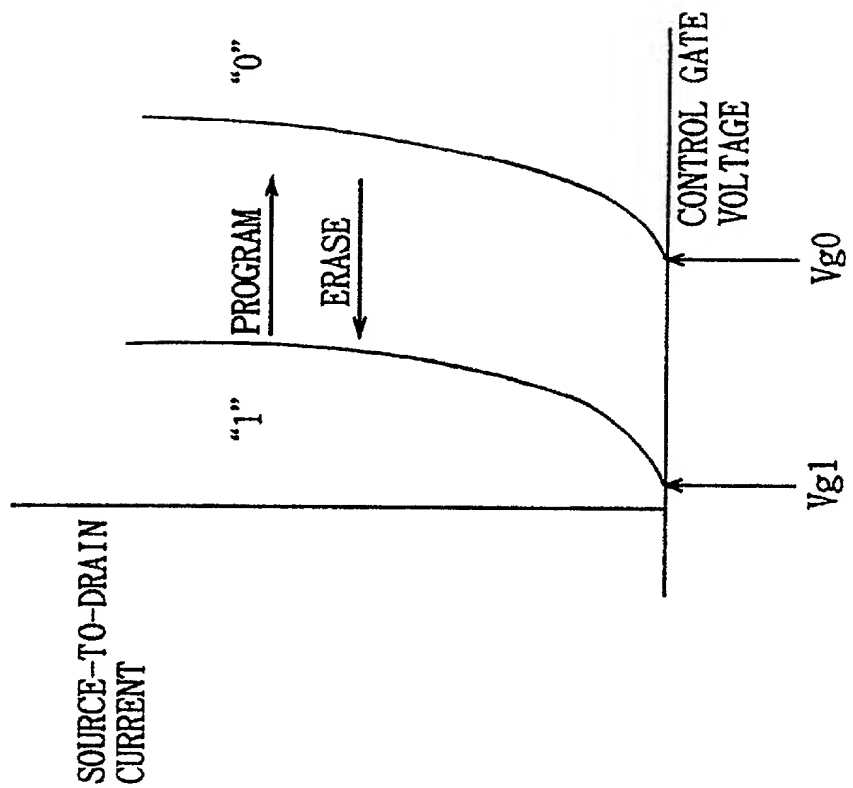

(PRIOR ART)
SOURCE-TO-DRAIN CURRENT
"1"
"0"
PROGRAM
ERASE
CONTROL GATE VOLTAGE
Vg1
Vg0

FIG. 2A (INVENTION)

	STORED DATA	FLOATING GATE	THRESHOLD VOLTAGE
ERASED STATE	"1"	INJECTION	HIGH
PROGRAMMED STATE	"0"	EMISSION	LOW

FIG. 2B (PRIOR ART)

	STORED DATA	FLOATING GATE	THRESHOLD VOLTAGE
ERASED STATE	"1"	EMISSION	LOW
PROGRAMMED STATE	"0"	INJECTION	HIGH

FIG. 3

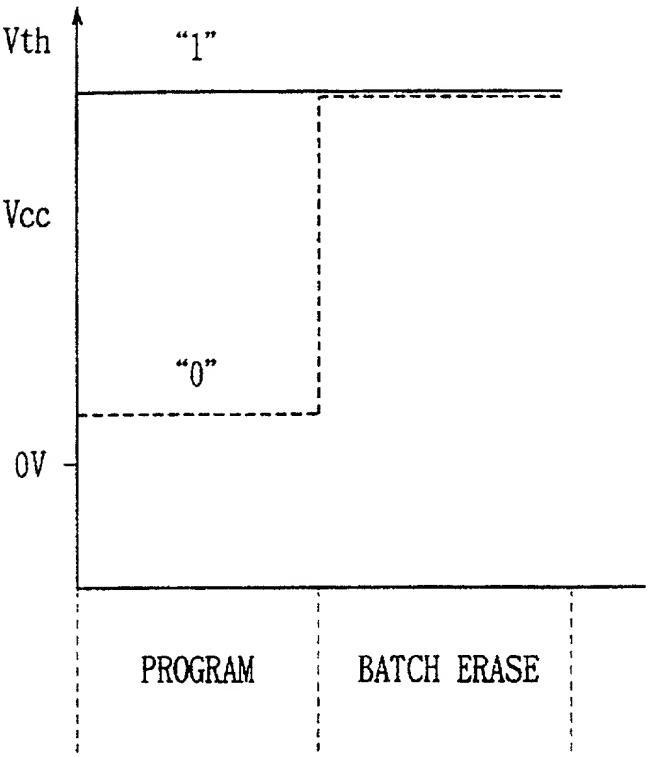

Vth
"1"
Vcc
"0"
0V
PROGRAM
BATCH ERASE

FIG. 4

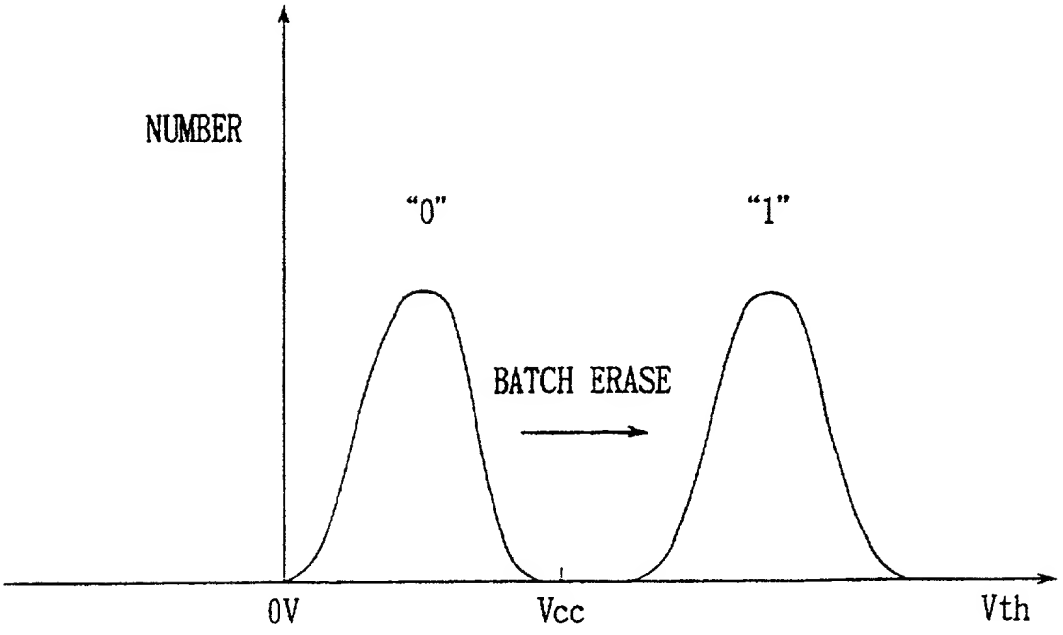

NUMBER
"0"
"1"
BATCH ERASE
0V
Vcc
Vth

FIG. 5

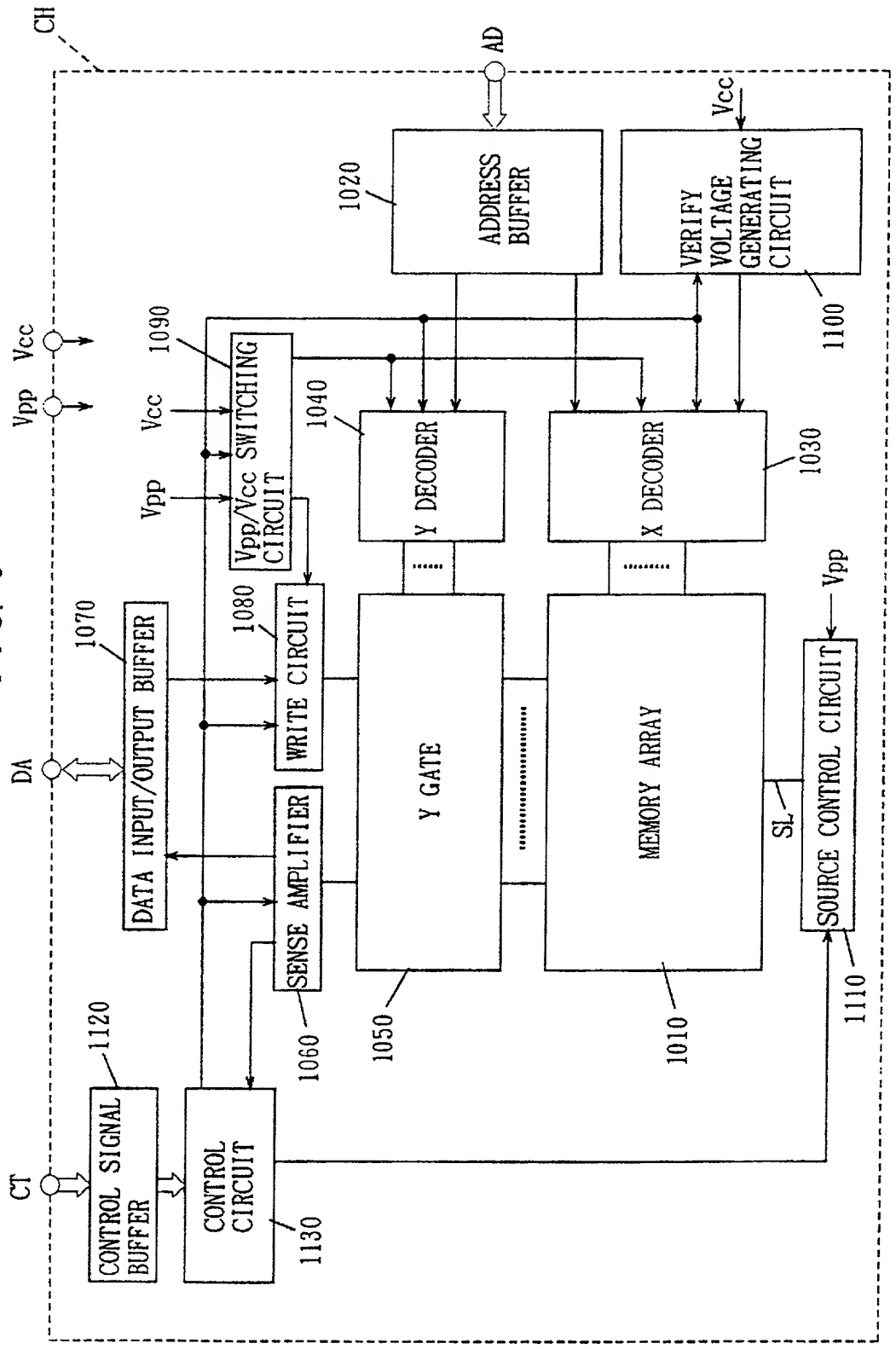
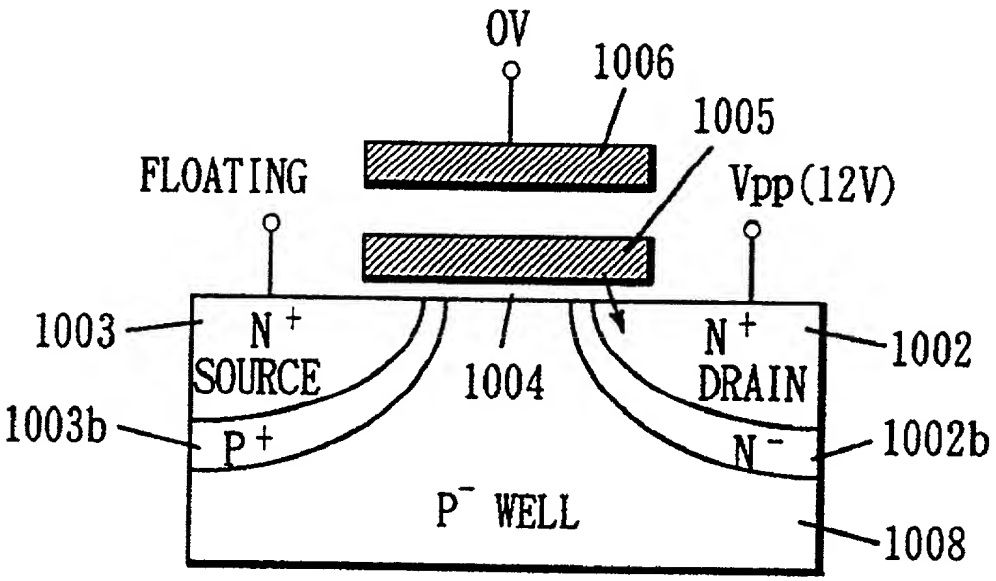

CH
AD
Vcc
ADDRESS BUFFER
1020
VERIFY VOLTAGE GENERATING CIRCUIT
1100
Vpp Vcc
1090
Vcc
Vpp
Vpp/Vcc SWITCHING CIRCUIT
1040
Y DECODER
X DECODER
1030
1070
1080
DA
DATA INPUT/OUTPUT BUFFER
WRITE CIRCUIT
Y GATE
MEMORY ARRAY
Vpp
SL
SOURCE CONTROL CIRCUIT
1110
SENSE AMPLIFIER
1060
1050
1010
1120
CT
CONTROL SIGNAL BUFFER
CONTROL CIRCUIT
1130

FIG. 6A

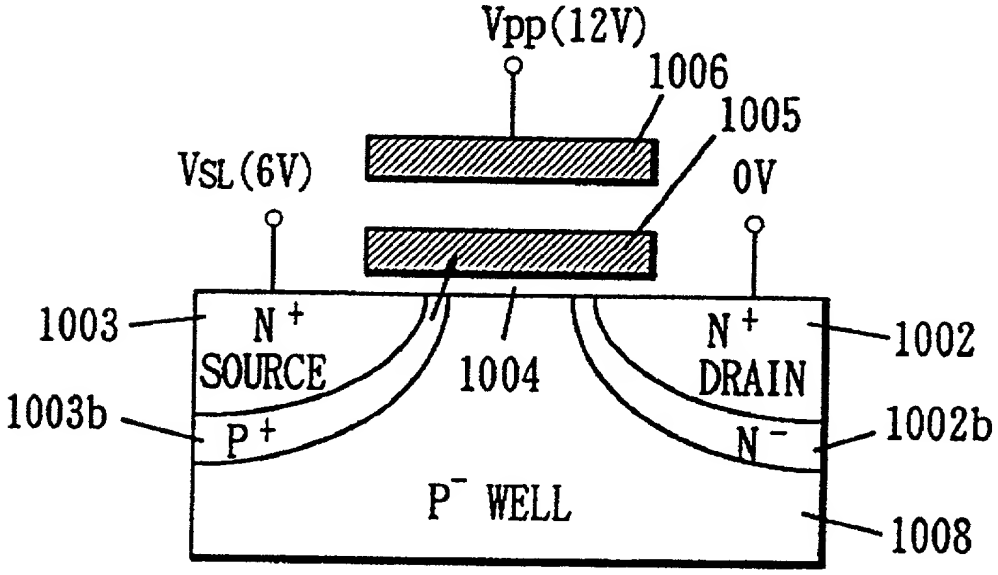
(PROGRAM)



〈TUNNEL EFFECT〉

FIG. 6B

(ERASE)



〈HOT ELECTRON〉

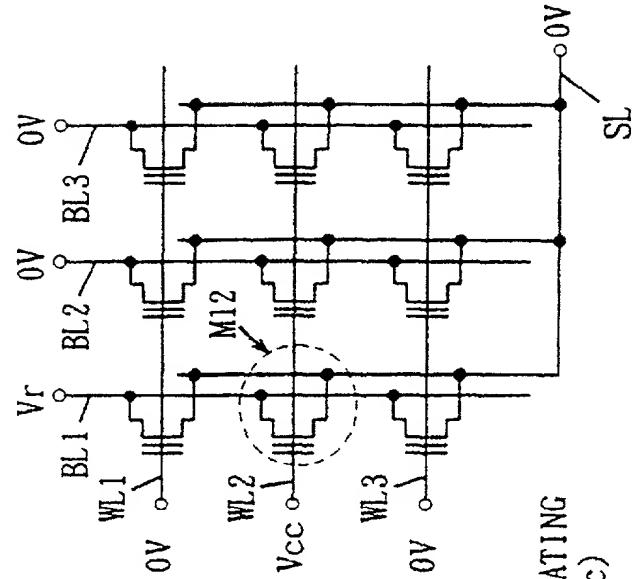


FIG. 7 (c)

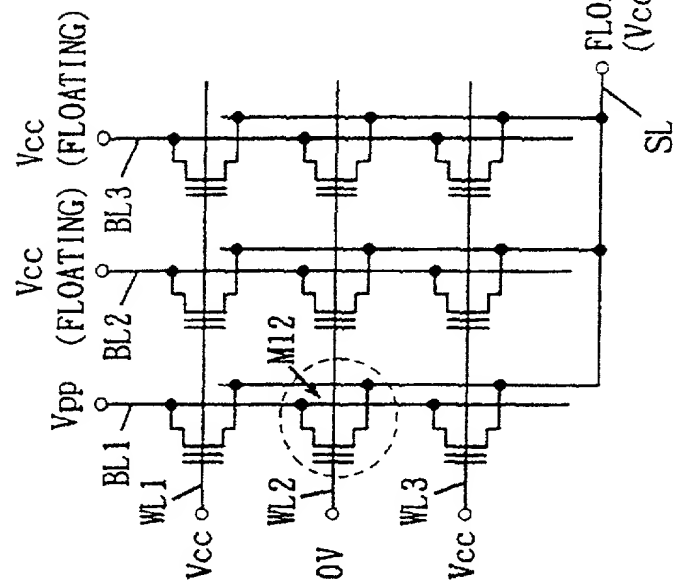


FIG. 7 (b)

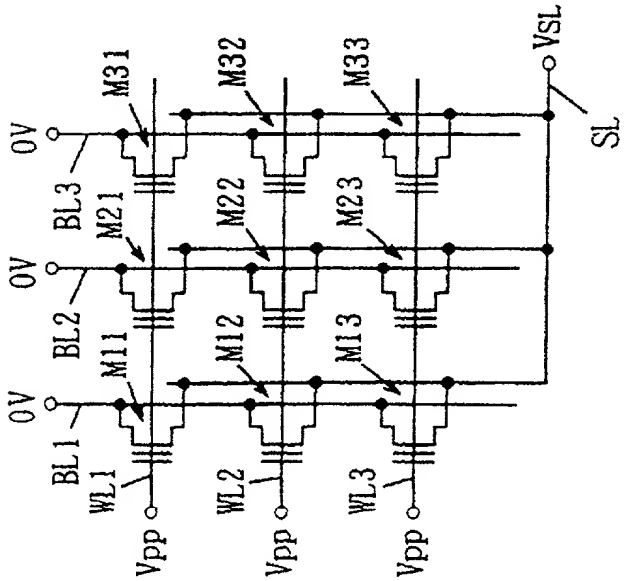
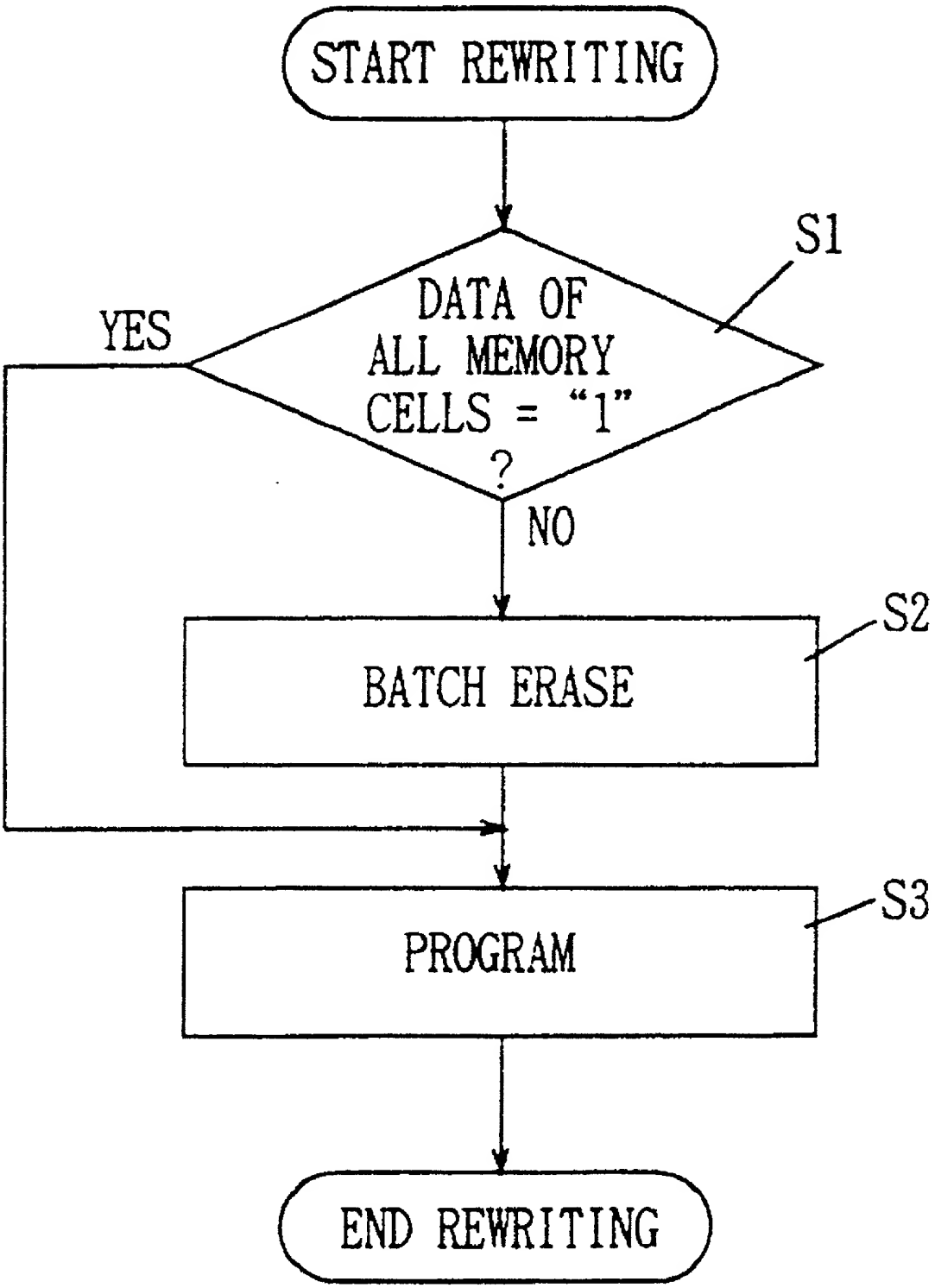


FIG. 7 (a)

FIG. 8


START REWRITING
S1
DATA OF ALL MEMORY CELLS = "1" ?
YES
NO
S2
BATCH ERASE
S3
PROGRAM
END REWRITING

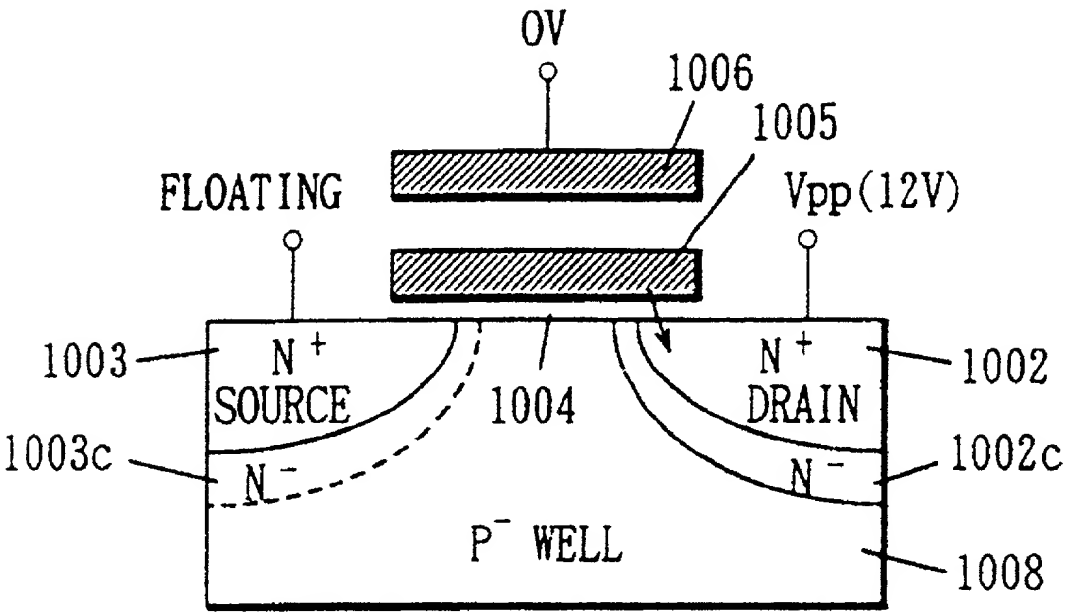

0V
1006
1005
FLOATING
Vpp(12V)
1003
N+
SOURCE
1004
N+
DRAIN
1002
1003c
N-
N-
1002c
P- WELL
1008

FIG. 9 (a)

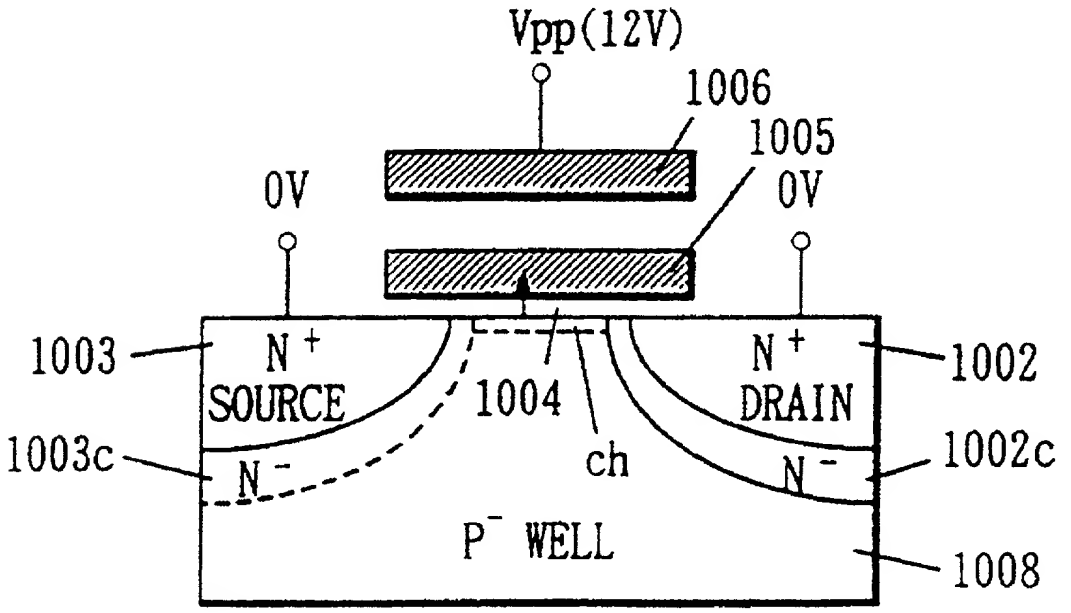

Vpp(12V)
1006
1005
0V
0V
1003
N+
SOURCE
1004
ch
N+
DRAIN
1002
1003c
N-
N-
1002c
P- WELL
1008

FIG. 9 (b)

FIG. 10A

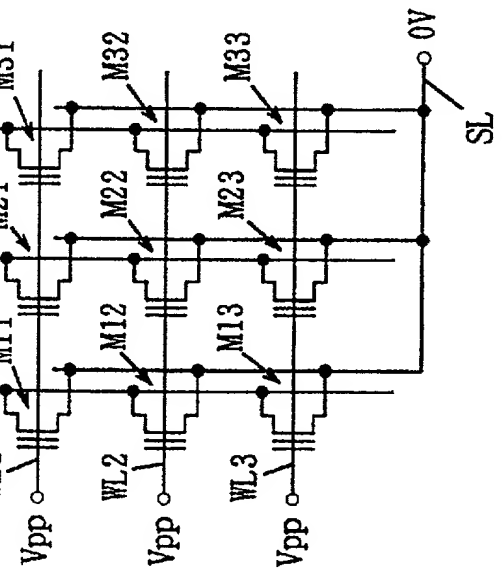


FIG. 10B

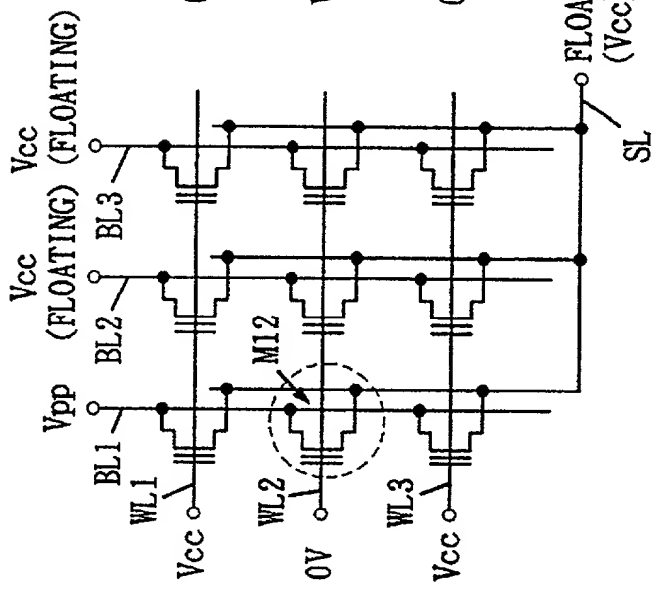
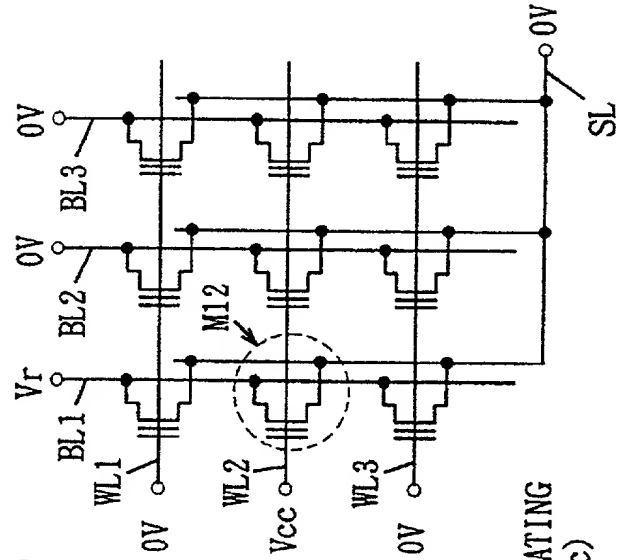


FIG. 10C



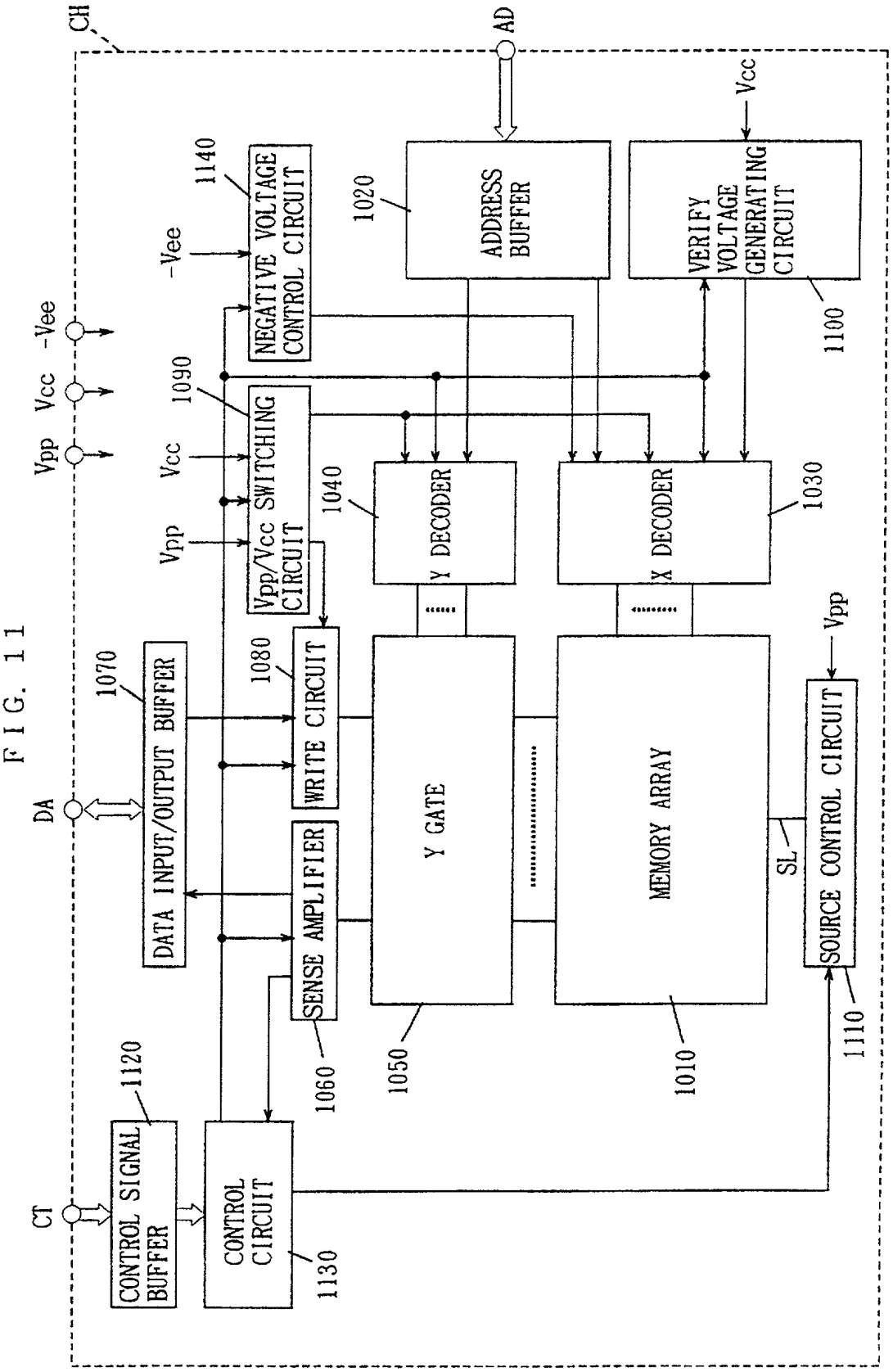

CH
AD
Vcc
-Vee
Vpp
Vcc
-Vee
1140
NEGATIVE VOLTAGE CONTROL CIRCUIT
1020
ADDRESS BUFFER
VERIFY VOLTAGE GENERATING CIRCUIT
1100
1090
Vpp/Vcc SWITCHING CIRCUIT
Vcc
Vpp
1040
Y DECODER
X DECODER
1030
1070
DATA INPUT/OUTPUT BUFFER
1080
WRITE CIRCUIT
Y GATE
MEMORY ARRAY
Vpp
SL
SOURCE CONTROL CIRCUIT
DA
SENSE AMPLIFIER
1060
1050
1010
1110
1120
CONTROL SIGNAL BUFFER
CONTROL CIRCUIT
1130
CT

FIG. 11

FIG. 12

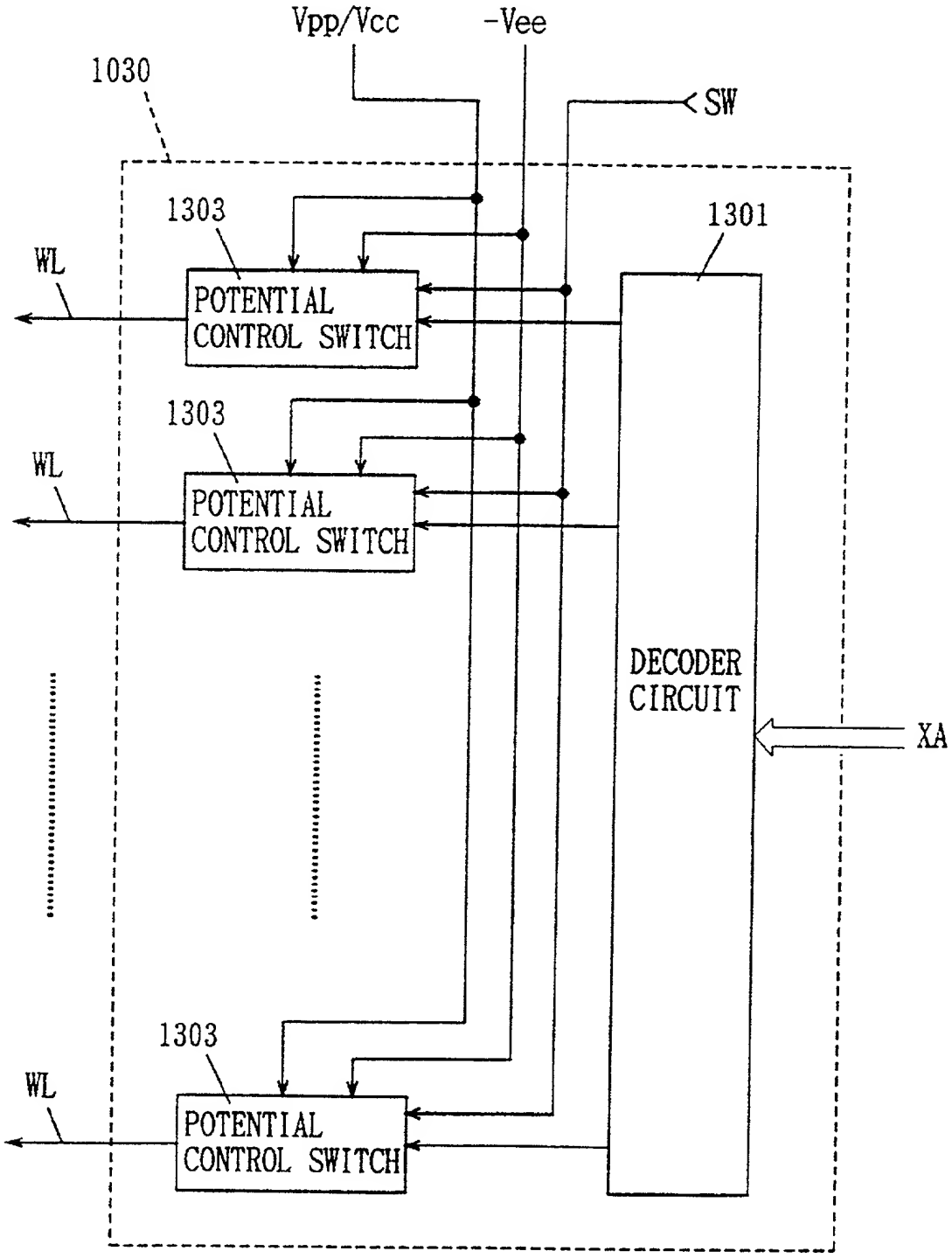
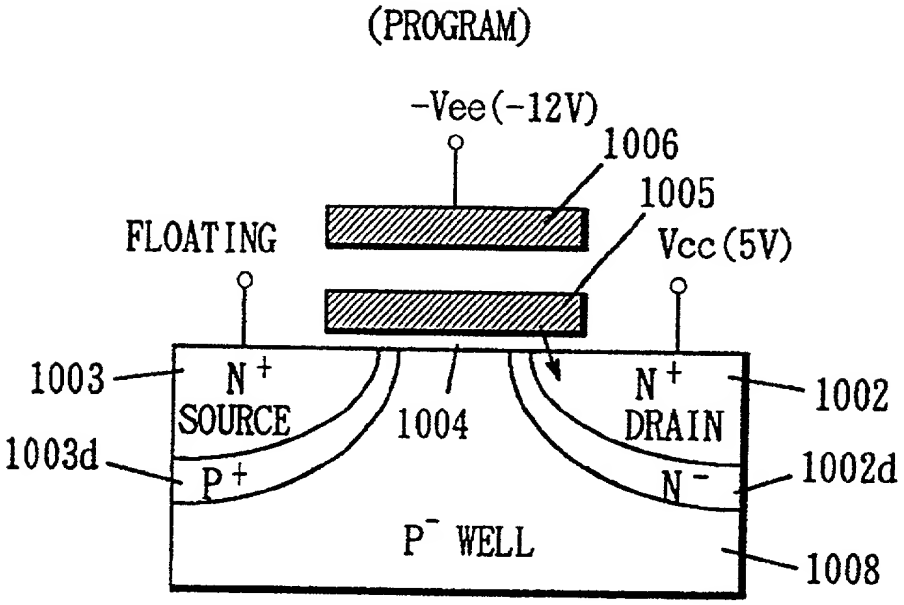
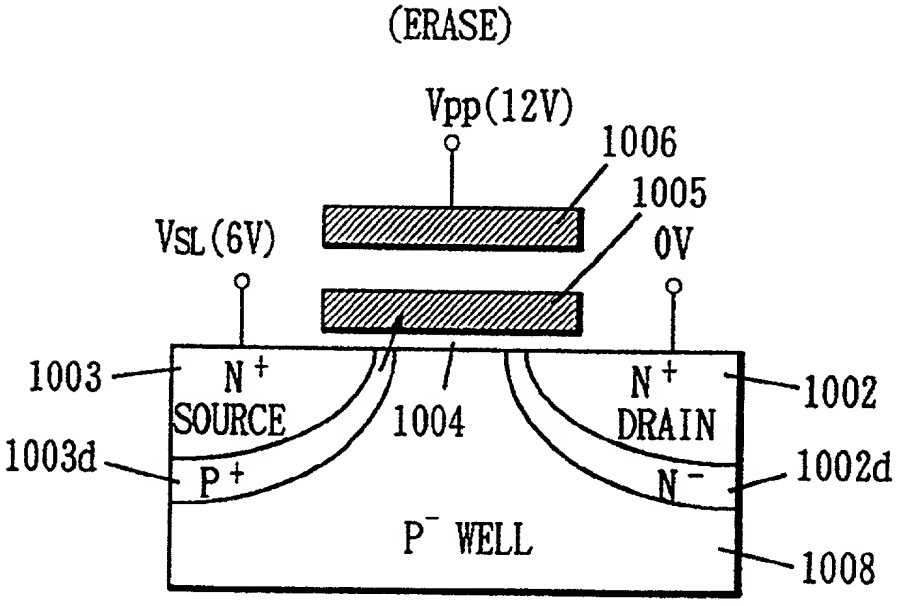

Vpp/Vcc
-Vee
1030
SW
1303
1301
WL
POTENTIAL CONTROL SWITCH
1303
WL
POTENTIAL CONTROL SWITCH
DECODER CIRCUIT
XA
1303
WL
POTENTIAL CONTROL SWITCH

FIG. 13A



〈TUNNEL EFFECT〉

FIG. 13B



〈HOT ELECTRON〉

FIG. 14A

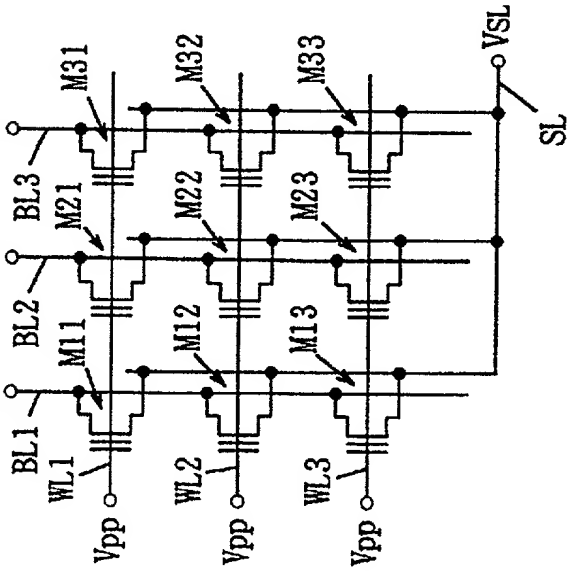


FIG. 14B

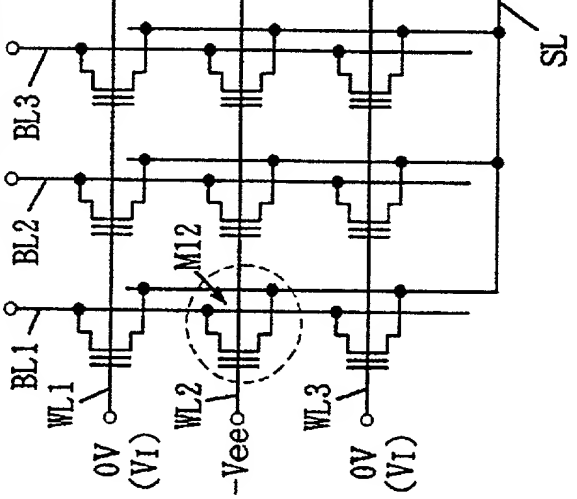


FIG. 14C

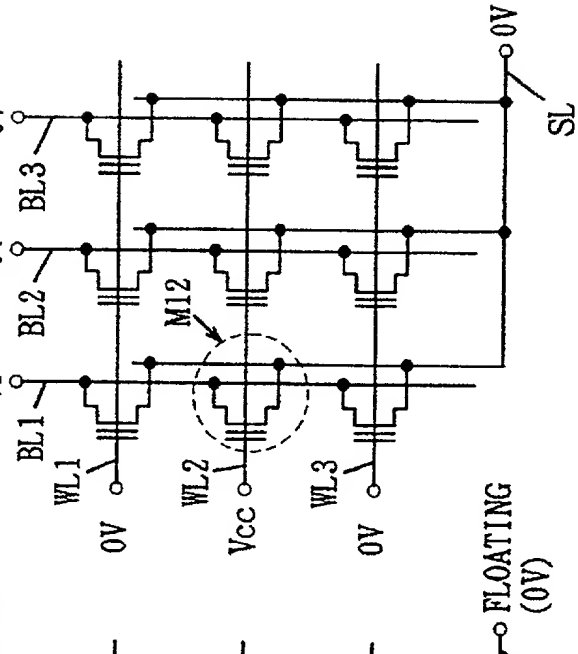


FIG. 15A

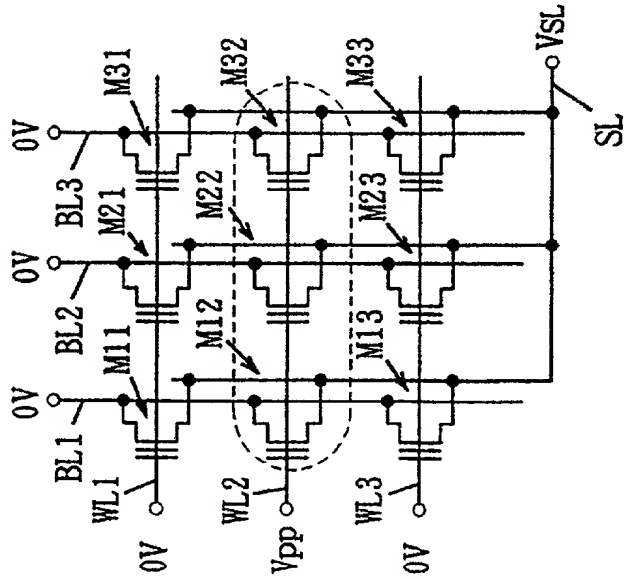


FIG. 15B

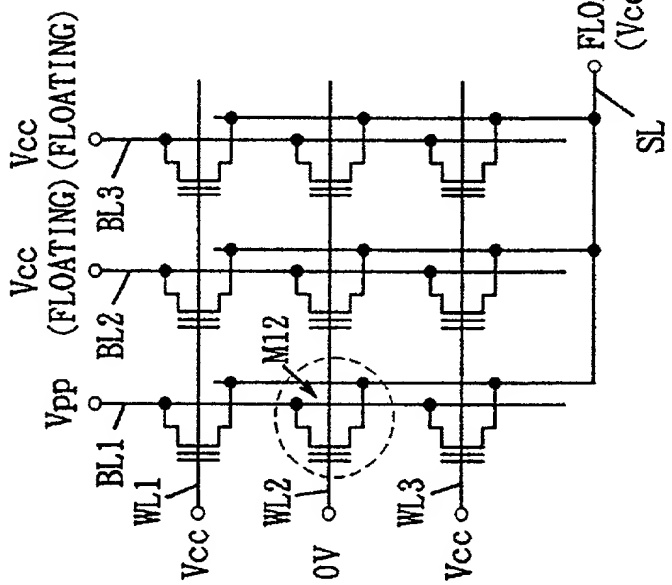


FIG. 15C

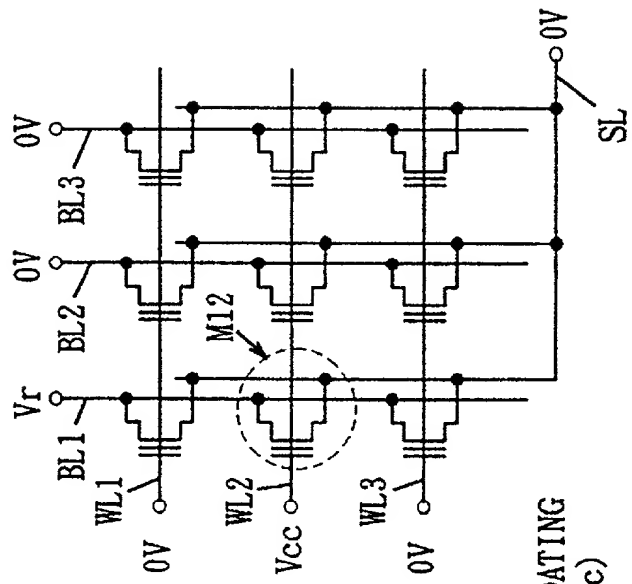


FIG. 16

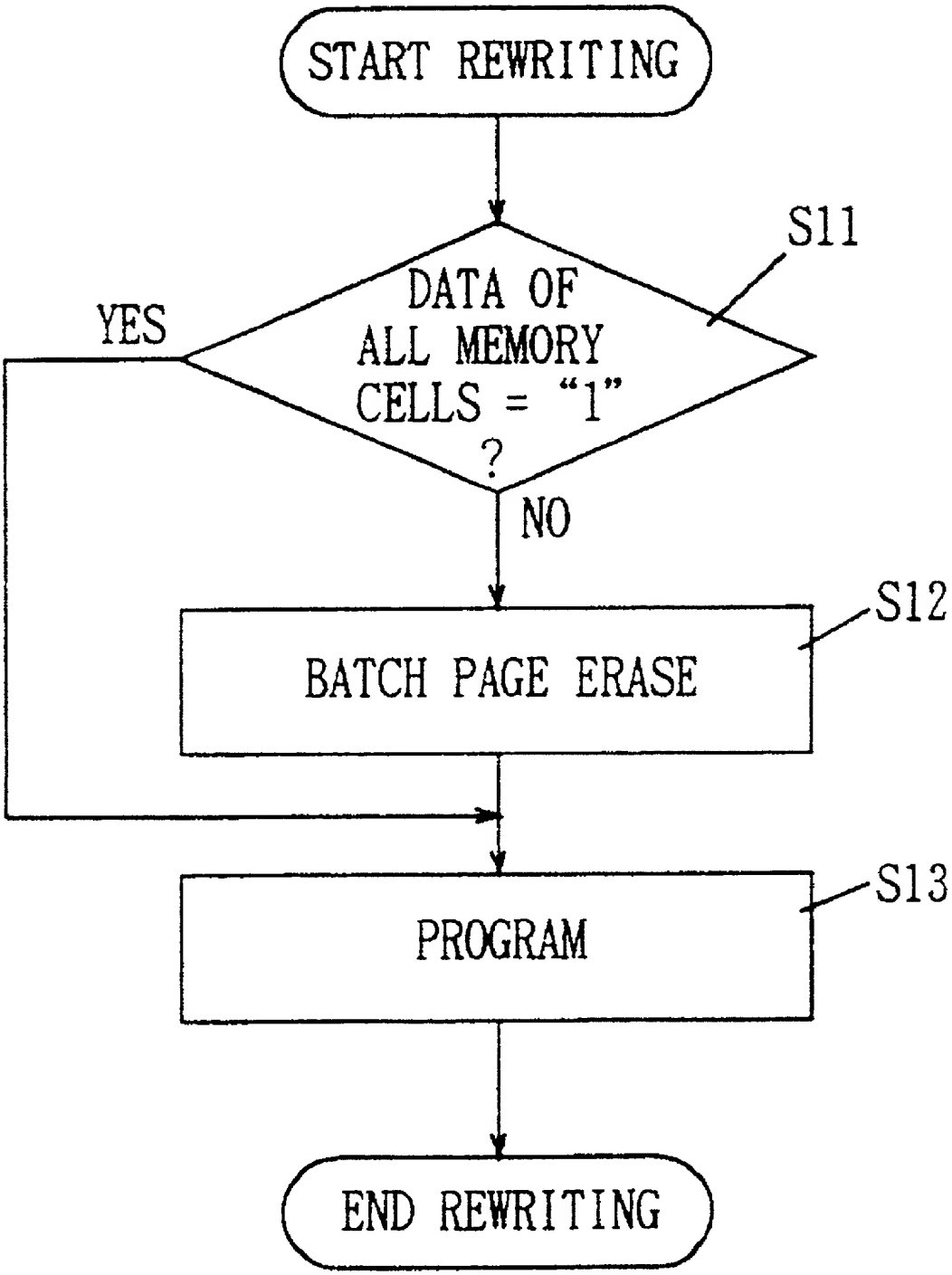

START REWRITING
S11
DATA OF ALL MEMORY CELLS = "1" ?
YES
NO
S12
BATCH PAGE ERASE
S13
PROGRAM
END REWRITING

FIG. 17A

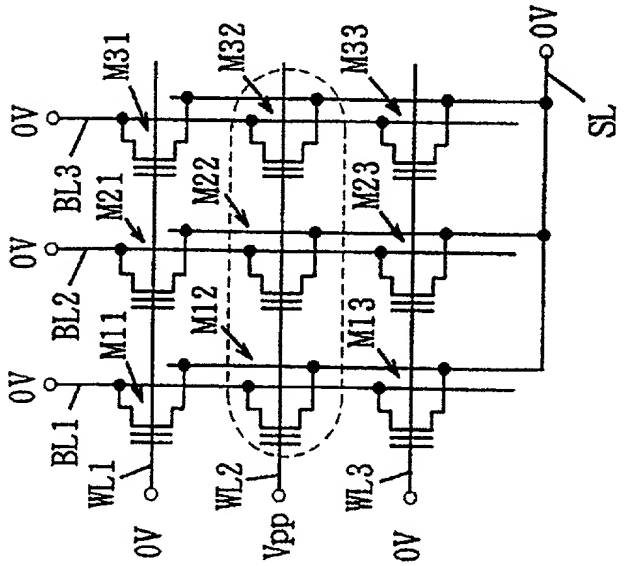


FIG. 17B

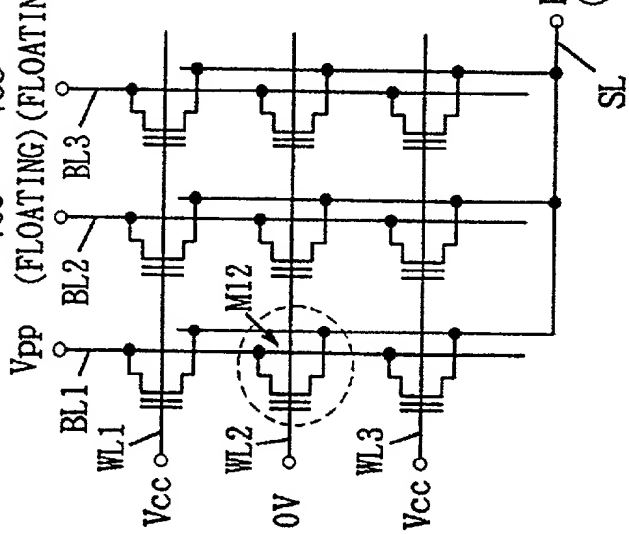
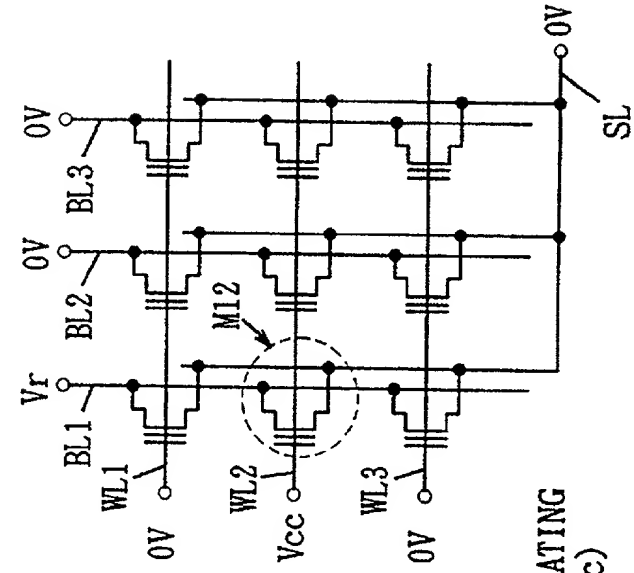


FIG. 17C



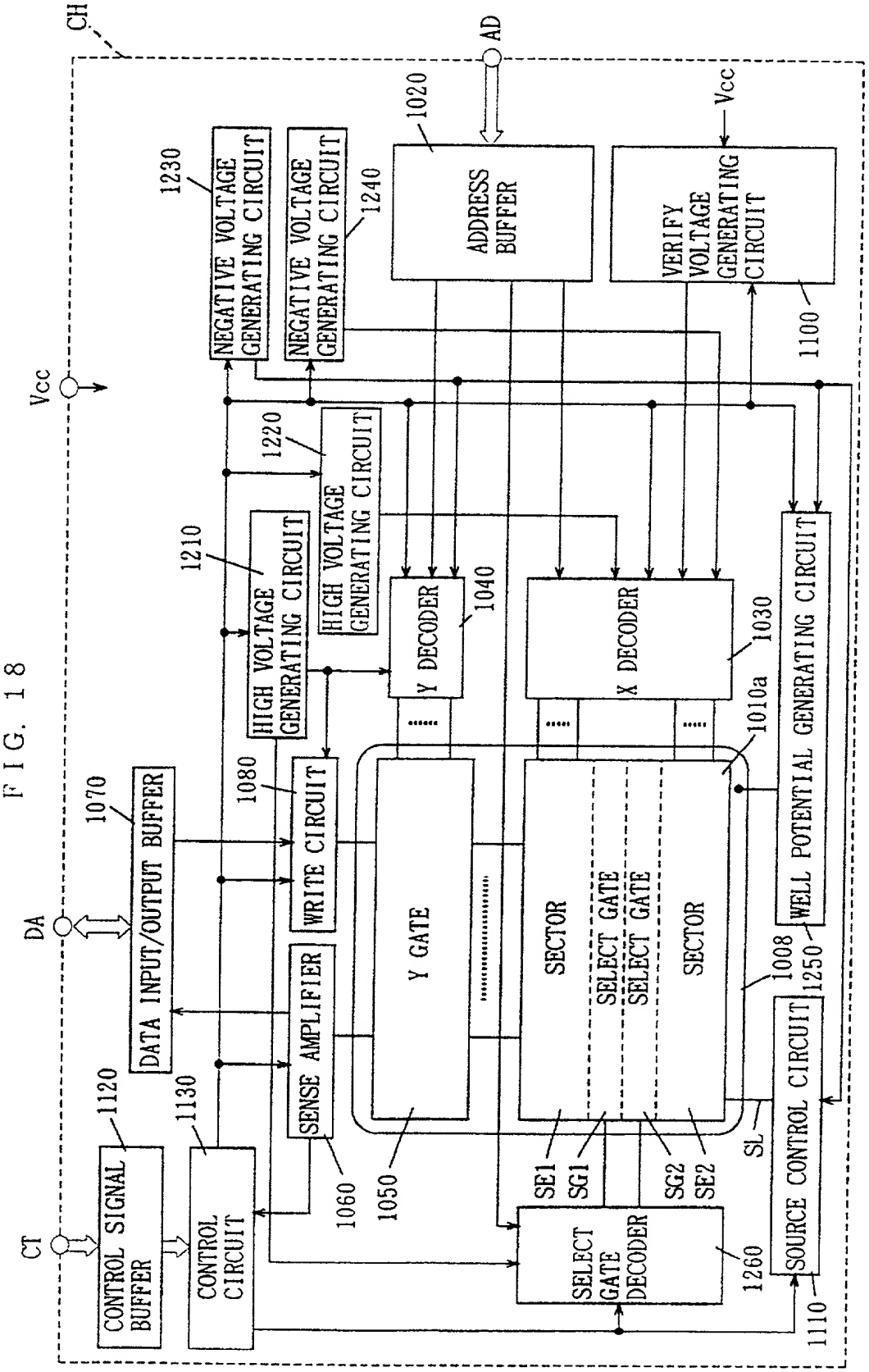

CH
AD
Vcc
1020
ADDRESS BUFFER
VERIFY VOLTAGE GENERATING CIRCUIT
1100
1230
NEGATIVE VOLTAGE GENERATING CIRCUIT
1240
NEGATIVE VOLTAGE GENERATING CIRCUIT
1220
HIGH VOLTAGE GENERATING CIRCUIT
1210
HIGH VOLTAGE GENERATING CIRCUIT
Y DECODER
1040
X DECODER
1030
1010a
WELL POTENTIAL GENERATING CIRCUIT
1070
DATA INPUT/OUTPUT BUFFER
1080
WRITE CIRCUIT
SENSE AMPLIFIER
Y GATE
SECTOR
SELECT GATE
SELECT GATE
SECTOR
1008
1250
SOURCE CONTROL CIRCUIT
DA
CT
1120
CONTROL SIGNAL BUFFER
1130
CONTROL CIRCUIT
1060
1050
SE1
SG1
SG2
SE2
SL
SELECT GATE DECODER
1260
1110

FIG. 18

FIG. 19

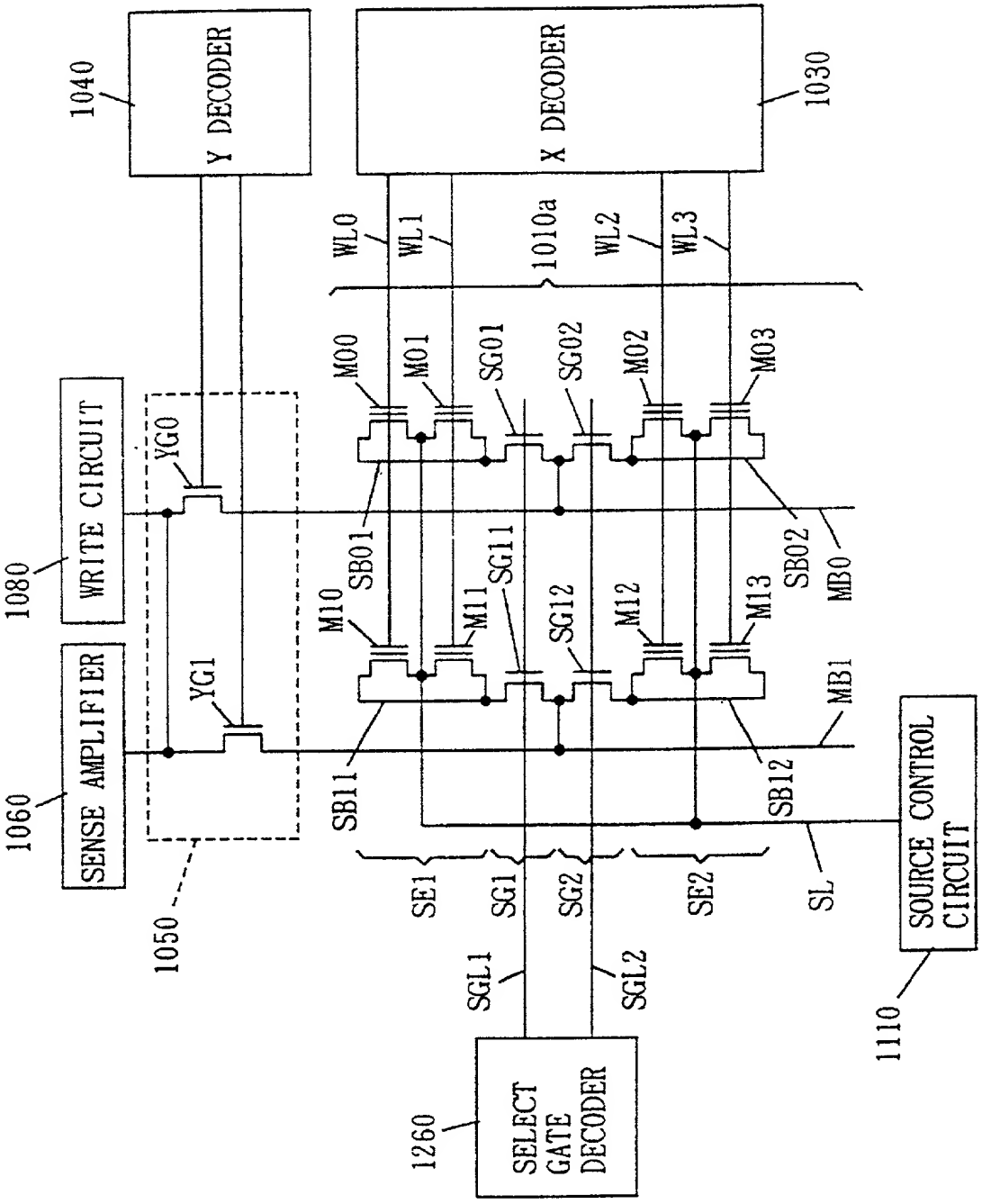
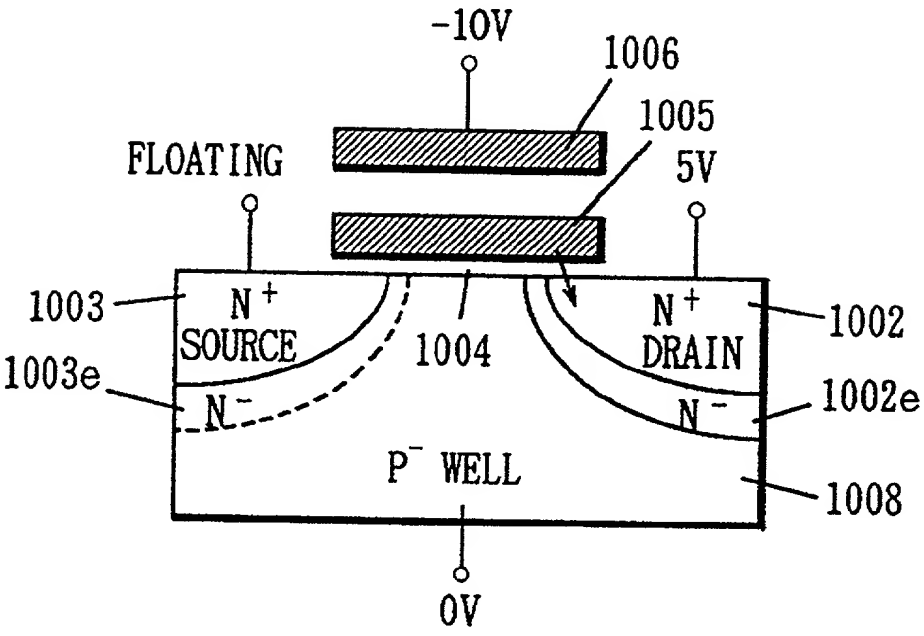
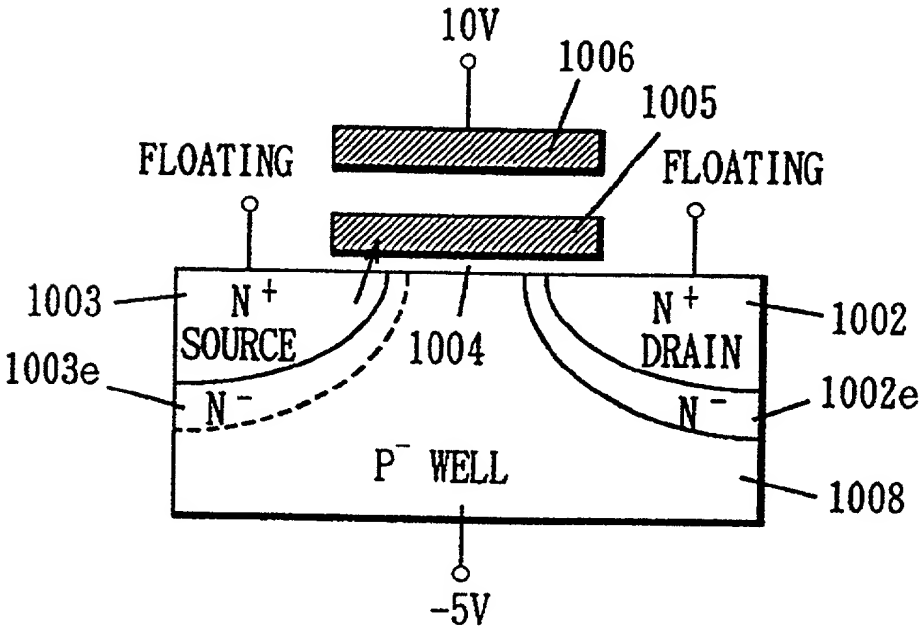

1040
Y DECODER
1030
X DECODER
1080
WRITE CIRCUIT
1060
SENSE AMPLIFIER
1050
YG0
YG1
WL0
WL1
1010a
WL2
WL3
M00
M01
SG01
SG02
M02
M03
SB01
SB02
MB0
M10
M11
SG11
SG12
M12
M13
MB1
SB11
SB12
SE1
SG1
SG2
SE2
SL
SGL1
SGL2
1260
SELECT GATE DECODER
1110
SOURCE CONTROL CIRCUIT

FIG. 20A



〈TUNNEL EFFECT〉

FIG. 20B



〈TUNNEL EFFECT〉

FIG. 21C

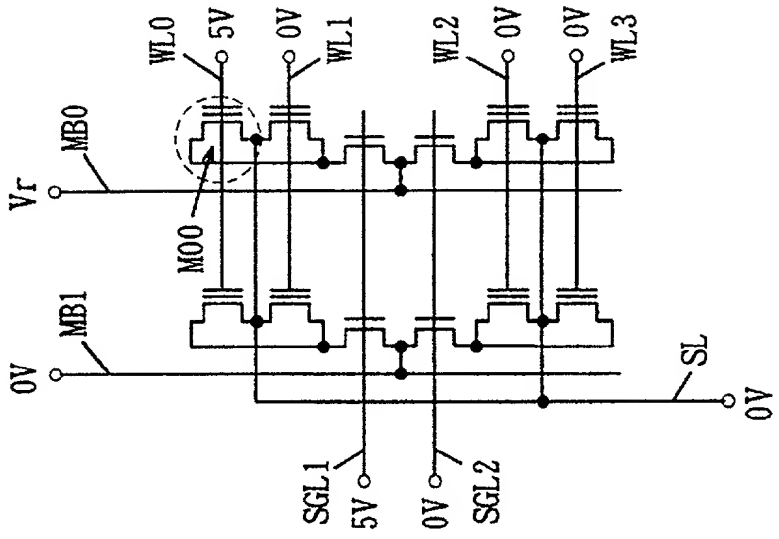


FIG. 21B

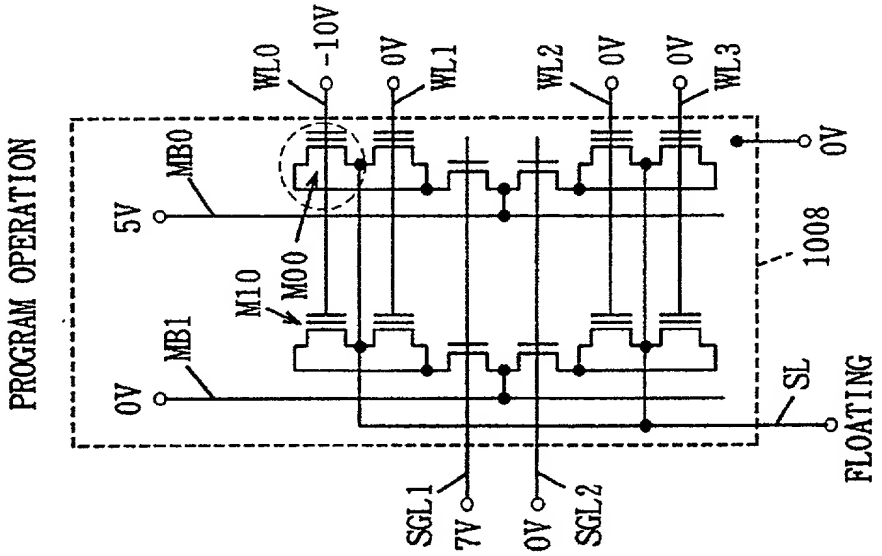


FIG. 21A

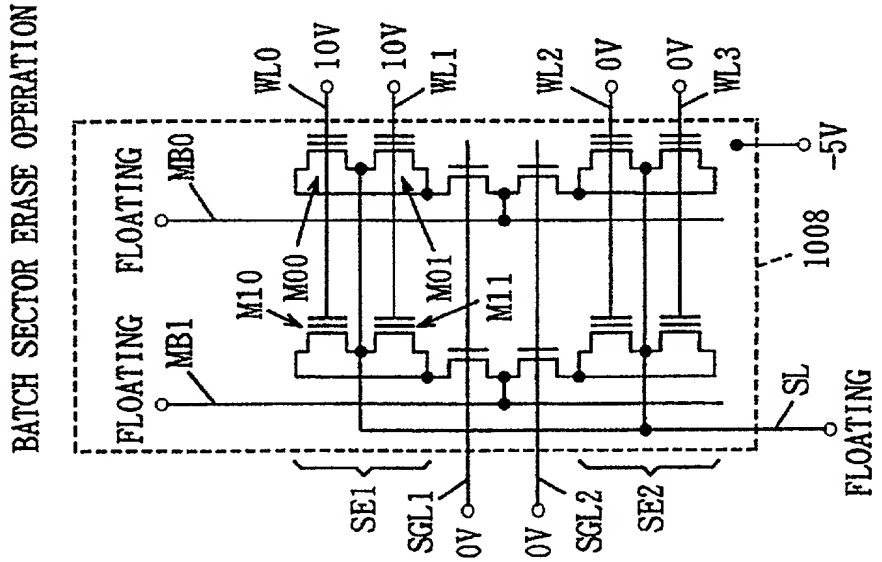
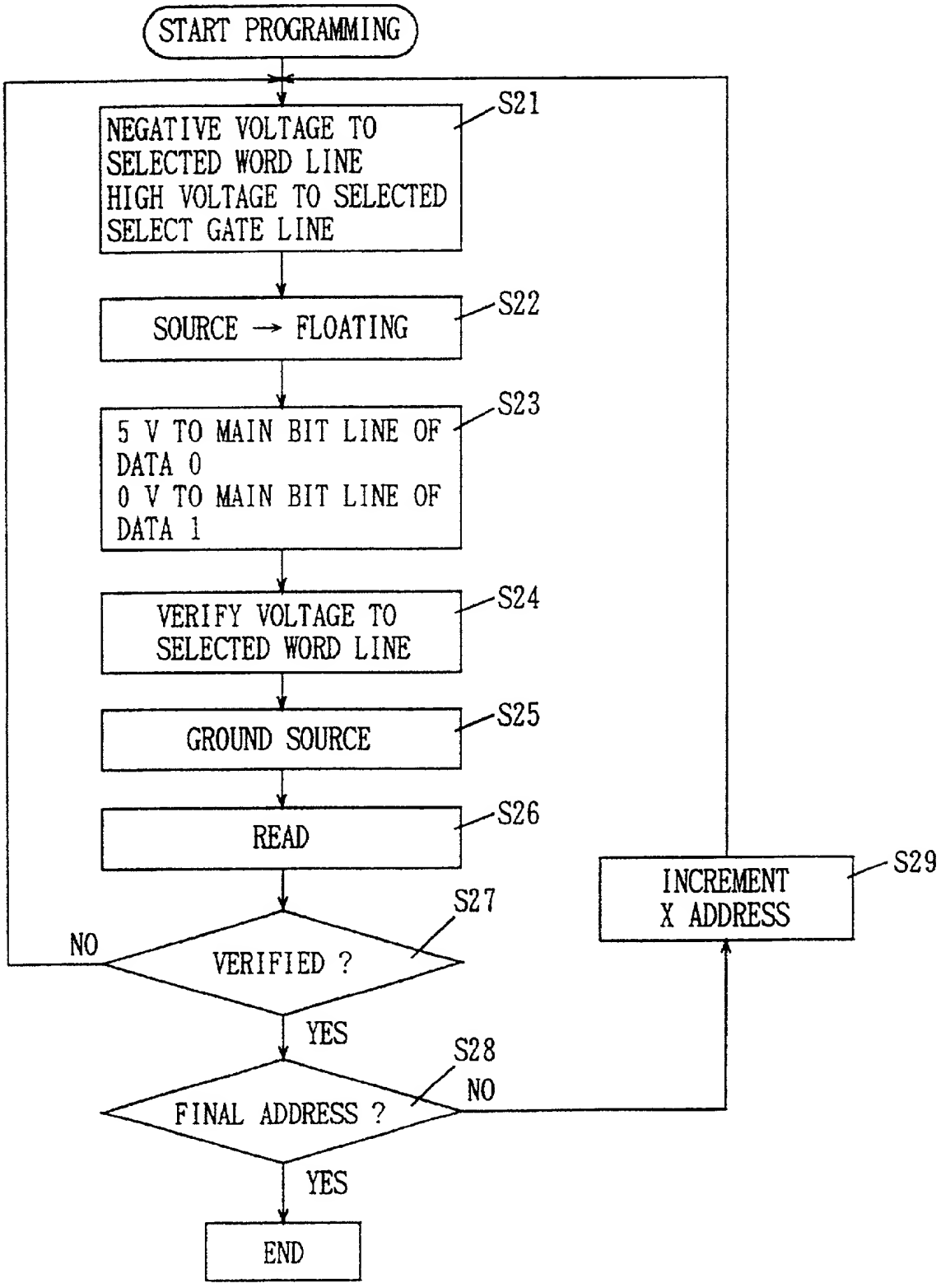


FIG. 22


START PROGRAMMING
NEGATIVE VOLTAGE TO SELECTED WORD LINE
HIGH VOLTAGE TO SELECTED SELECT GATE LINE
S21
SOURCE → FLOATING
S22
5 V TO MAIN BIT LINE OF DATA 0
0 V TO MAIN BIT LINE OF DATA 1
S23
VERIFY VOLTAGE TO SELECTED WORD LINE
S24
GROUND SOURCE
S25
READ
S26
VERIFIED ?
S27
NO
YES
FINAL ADDRESS ?
S28
NO
YES
INCREMENT X ADDRESS
S29
END

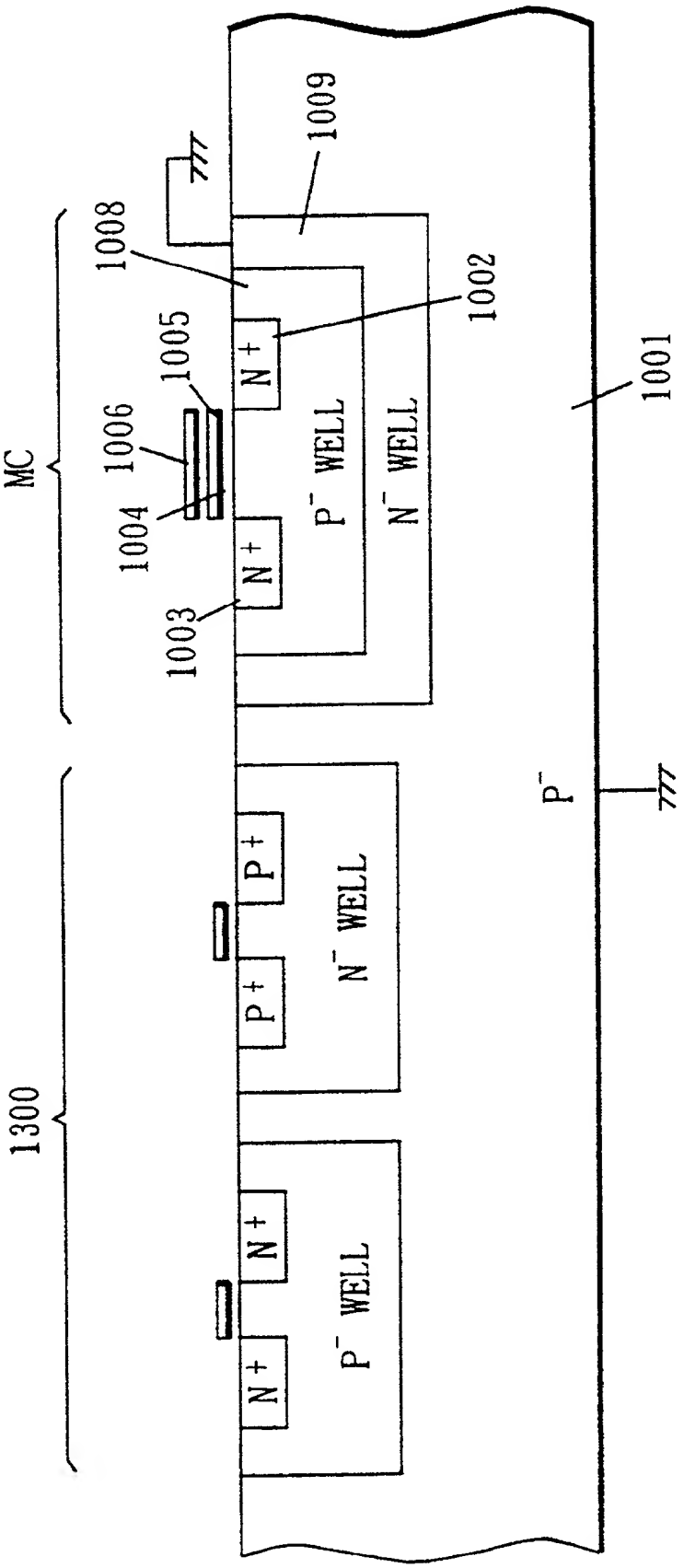

1009
1008
1002
1005
1006
1004
1003
MC
1001
N+
P⁻ WELL
N⁻ WELL
P+
P⁻
1300

FIG. 23

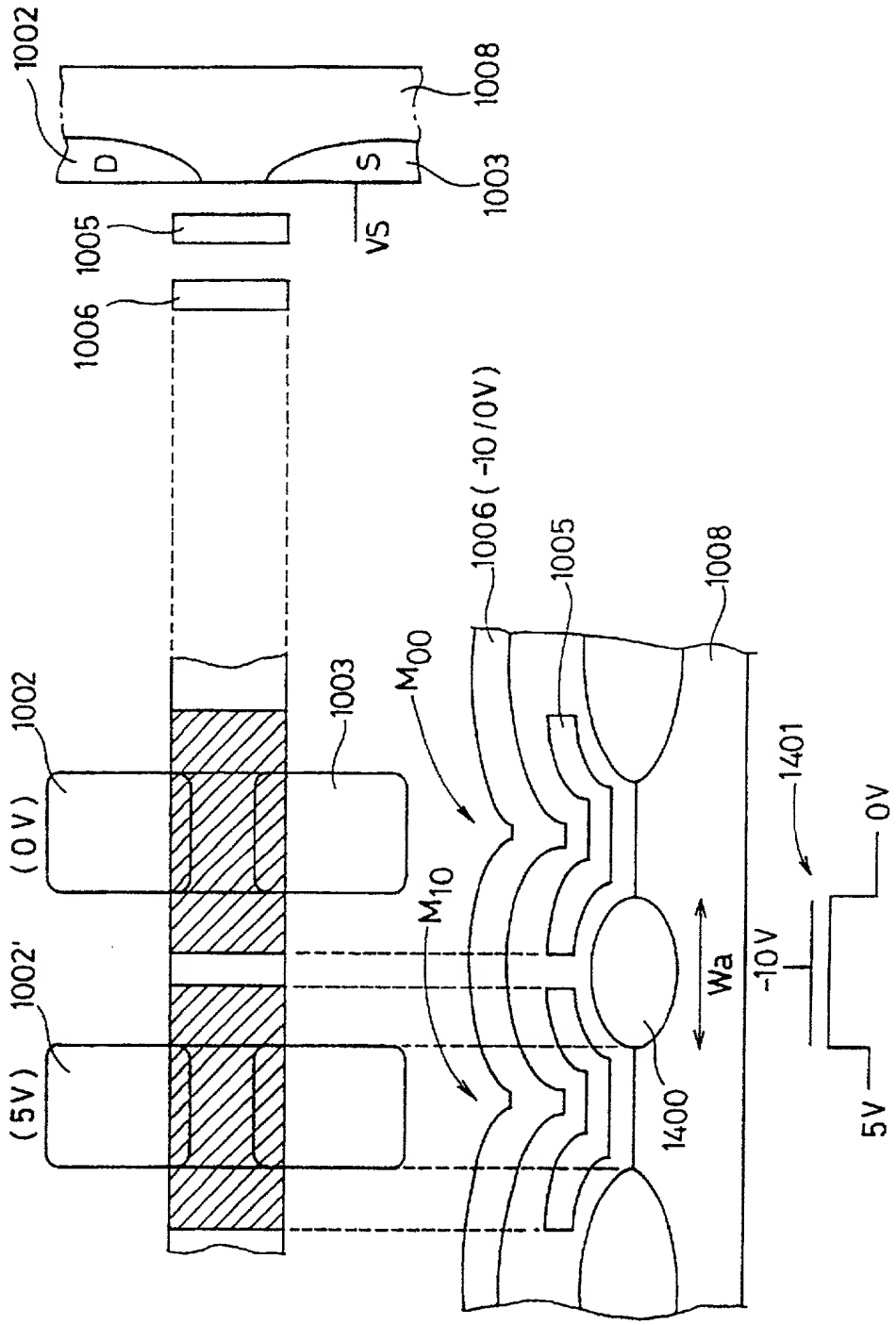

1002
1008
D
S
1003
VS
1005
1006
1006 (-10 / 0V)
1005
1008
1003
M_{00}
1002
(0 V)
M_{10}
1002'
(5V)
1401
0V
-10V
Wa
1400
5V

FIG. 24

FIG. 25

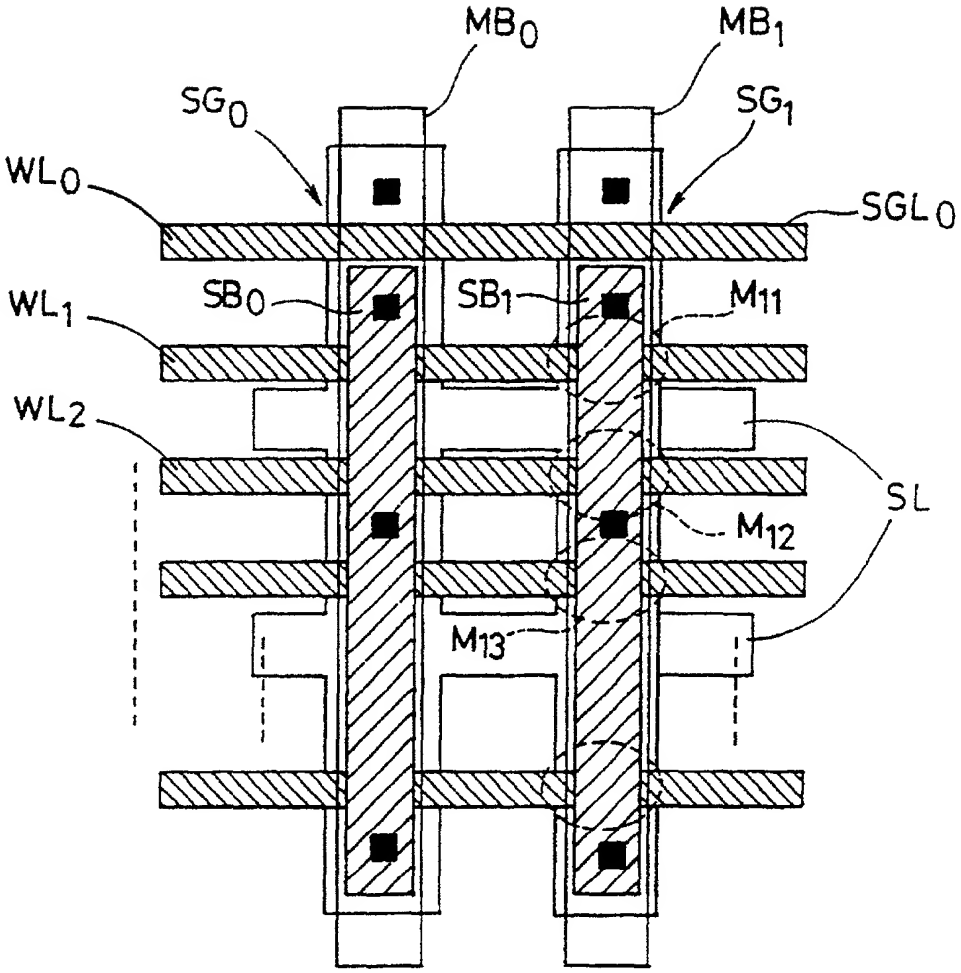


FIG. 26A

PROGRAM

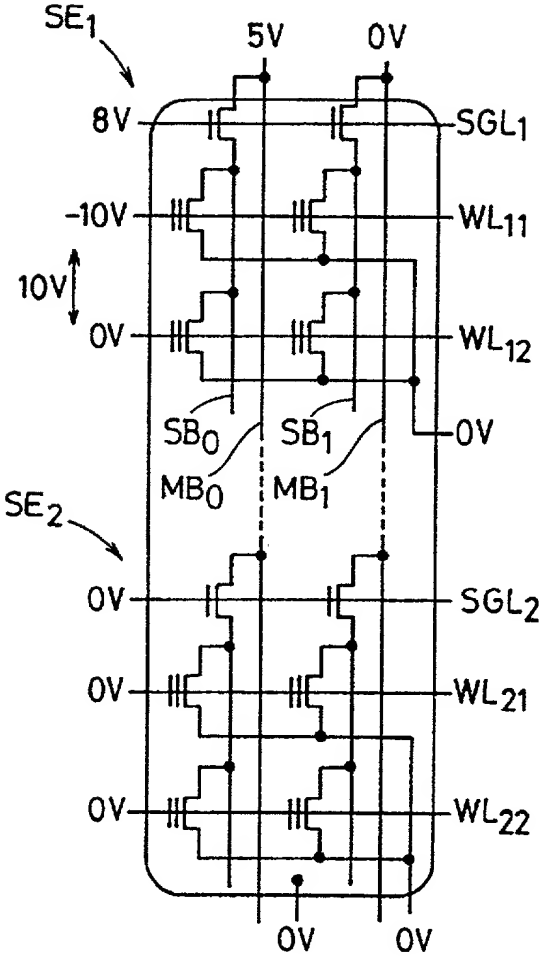


FIG. 26B

ERASE

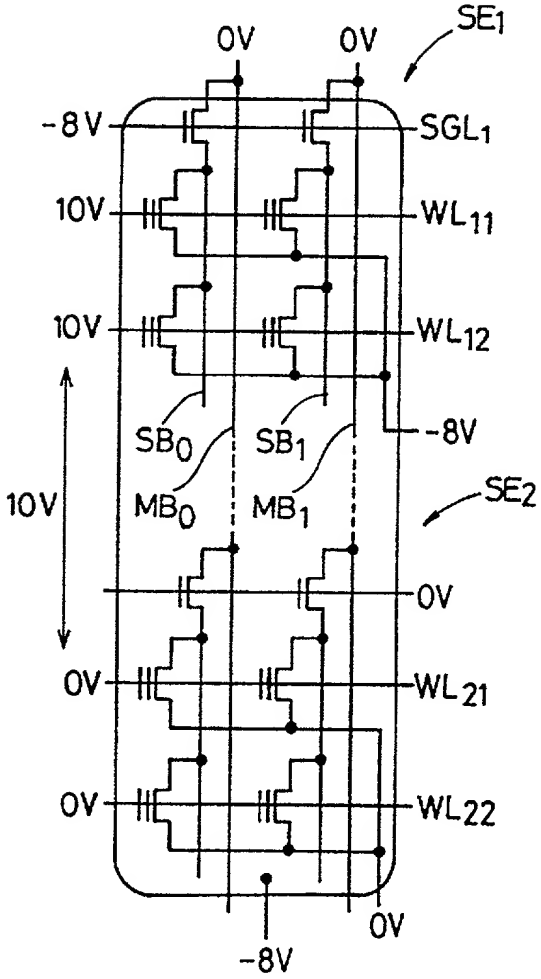


FIG. 27A

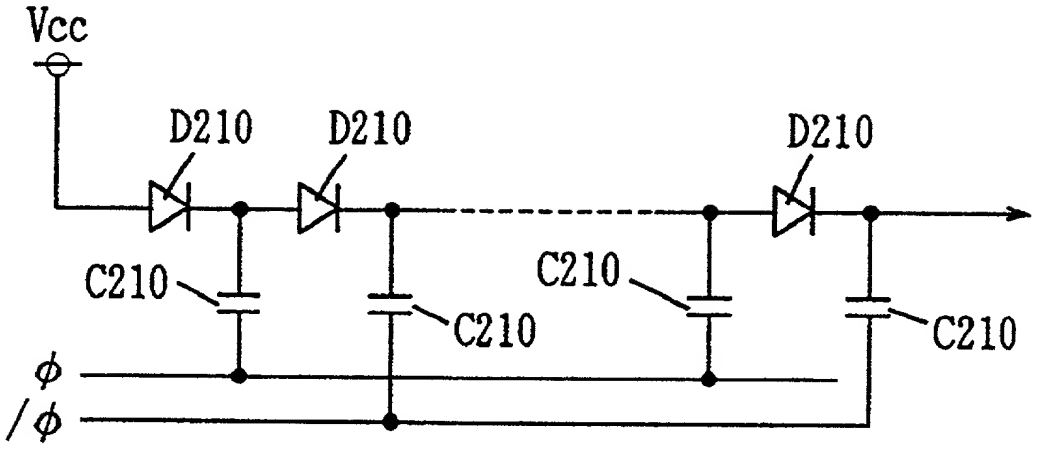


FIG. 27B

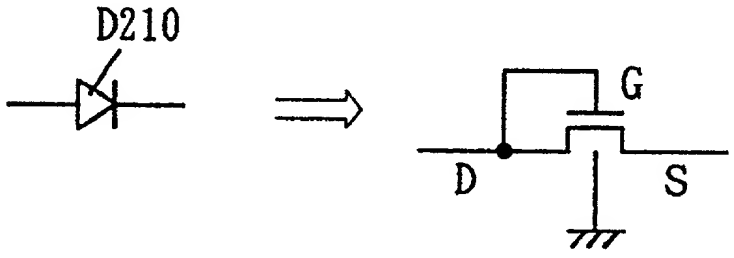


FIG. 28

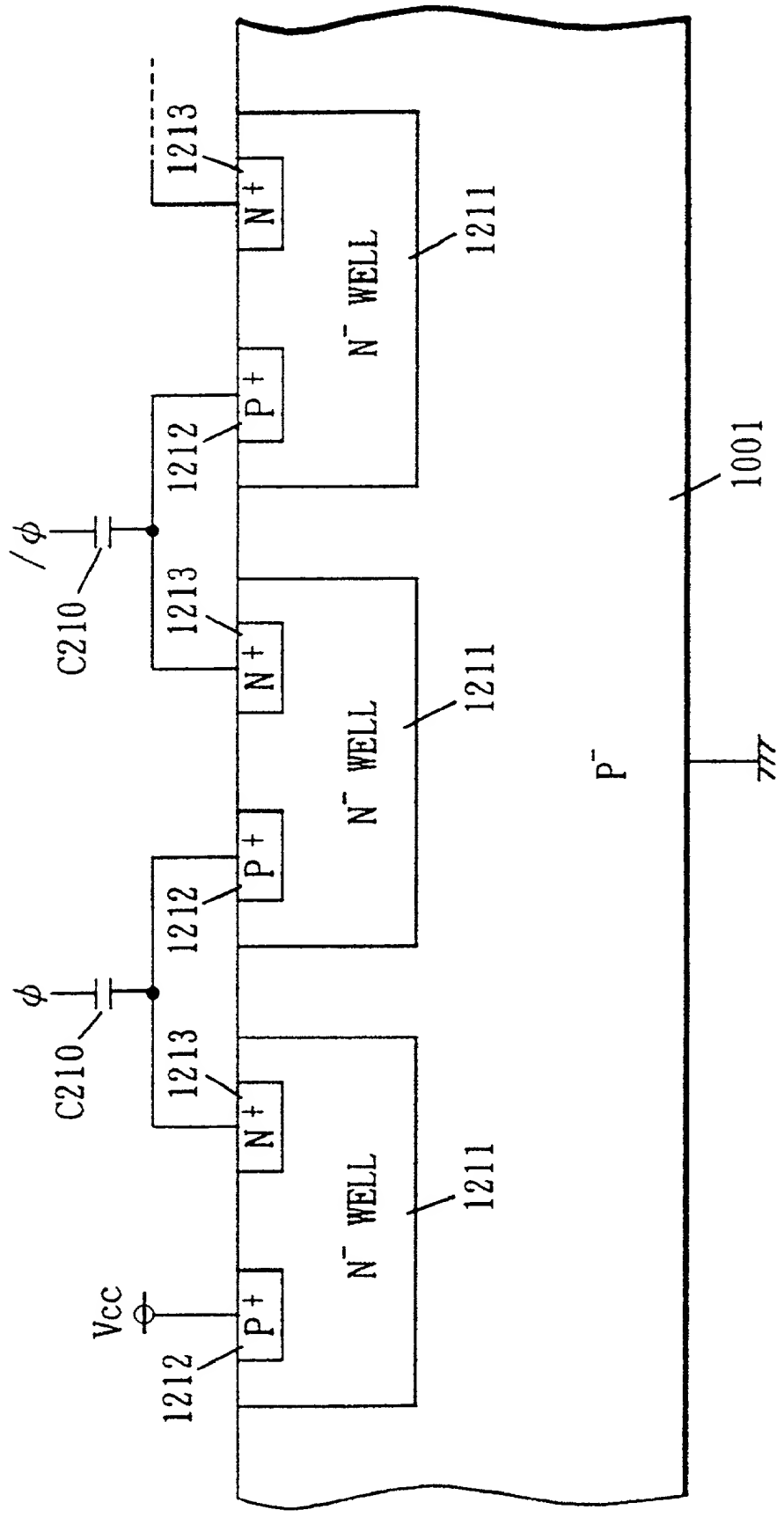

1213
N+
1211
N⁻ WELL
1212
P+
/φ
C210
1213
N+
1211
N⁻ WELL
1212
P+
φ
C210
1213
N+
1211
N⁻ WELL
Vcc
1212
P+
1001
P⁻

FIG. 29

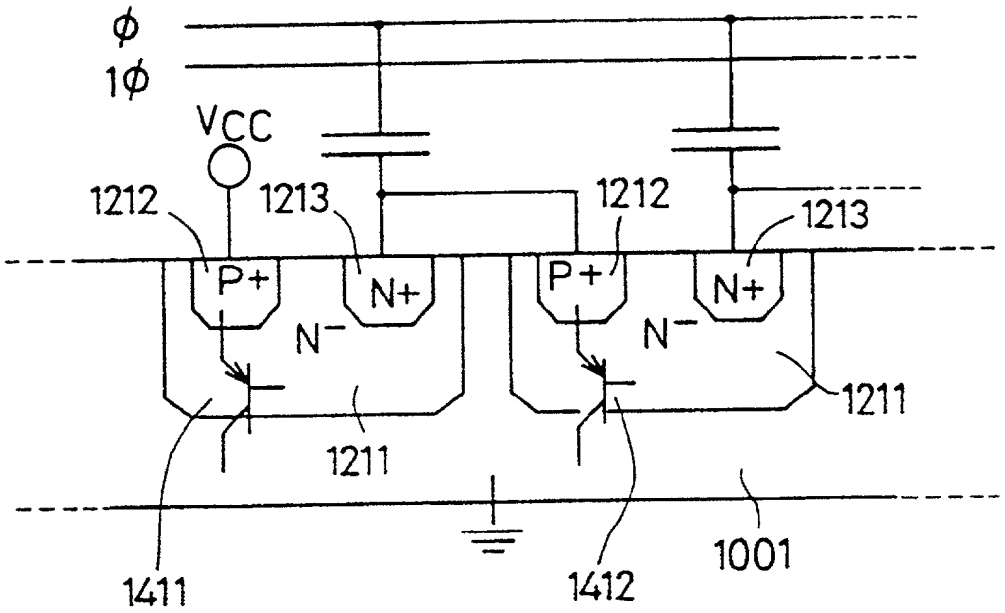

φ
1φ
VCC
1212
1213
1212
1213
P+
N+
P+
N+
N−
N−
1211
1211
1411
1412
1001

FIG. 30

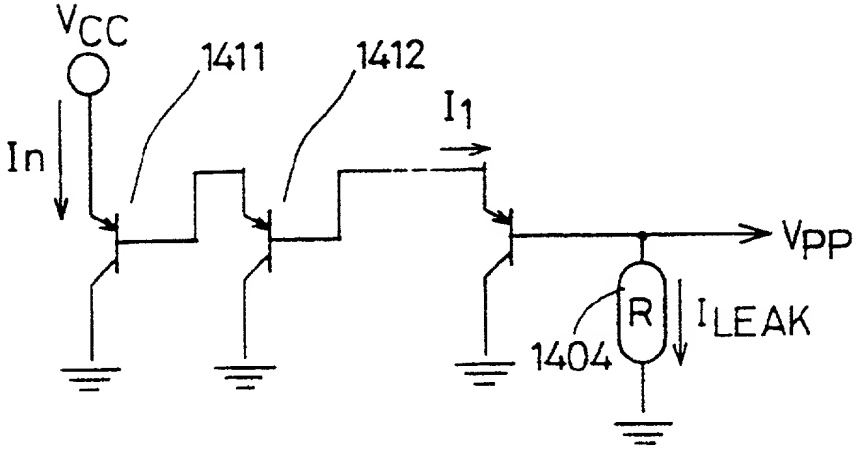

VCC
1411
1412
In
I1
VPP
R
ILEAK
1404

FIG. 31

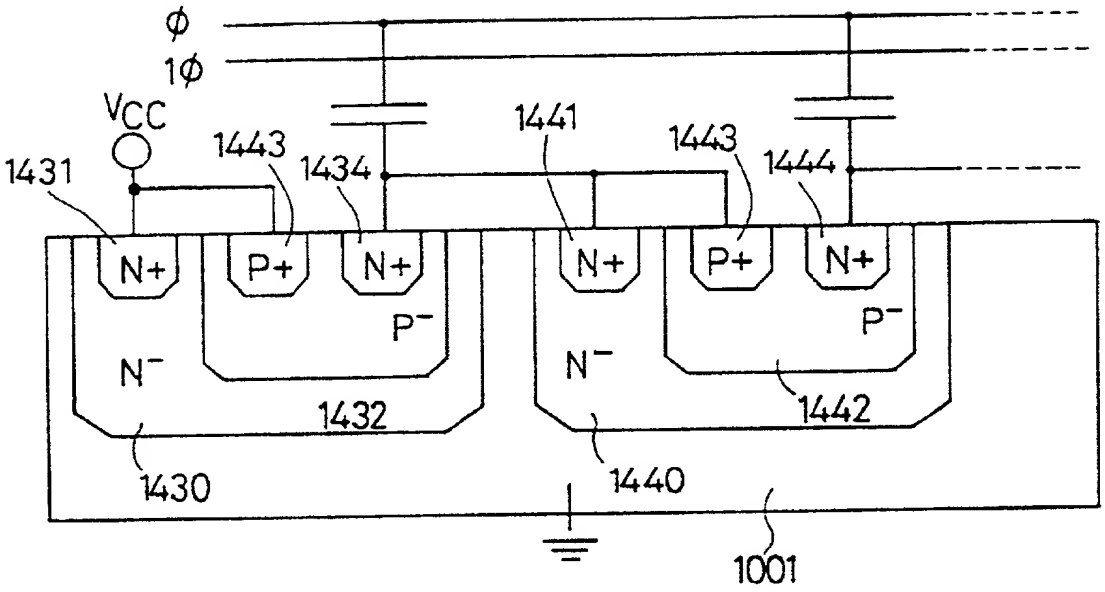

φ
1φ
VCC
1431
1443
1434
1441
1443
1444
N+
P+
N+
N+
P+
N+
P⁻
P⁻
N⁻
N⁻
1432
1442
1430
1440
1001

FIG. 32A

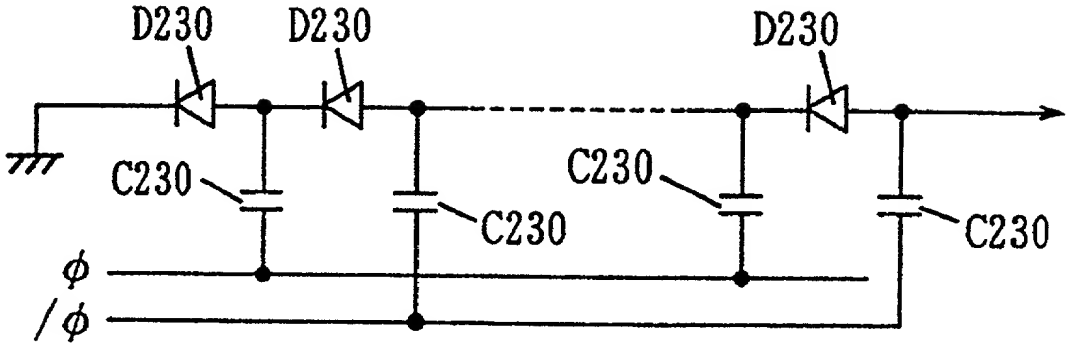


FIG. 32B

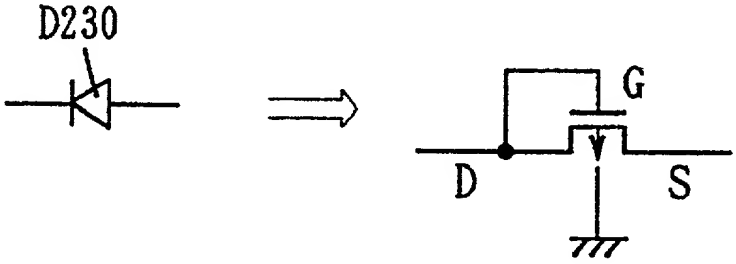
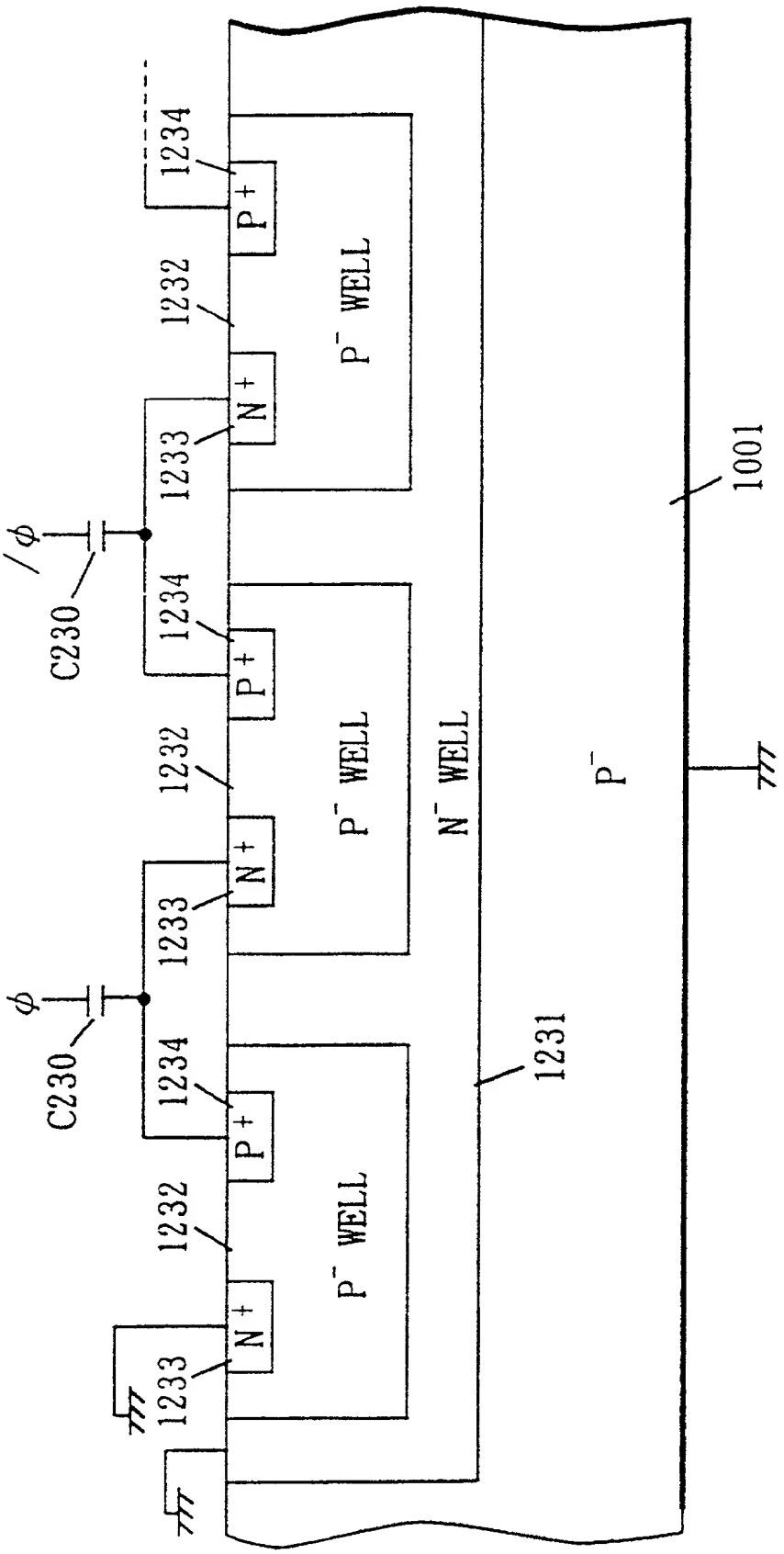


FIG. 33



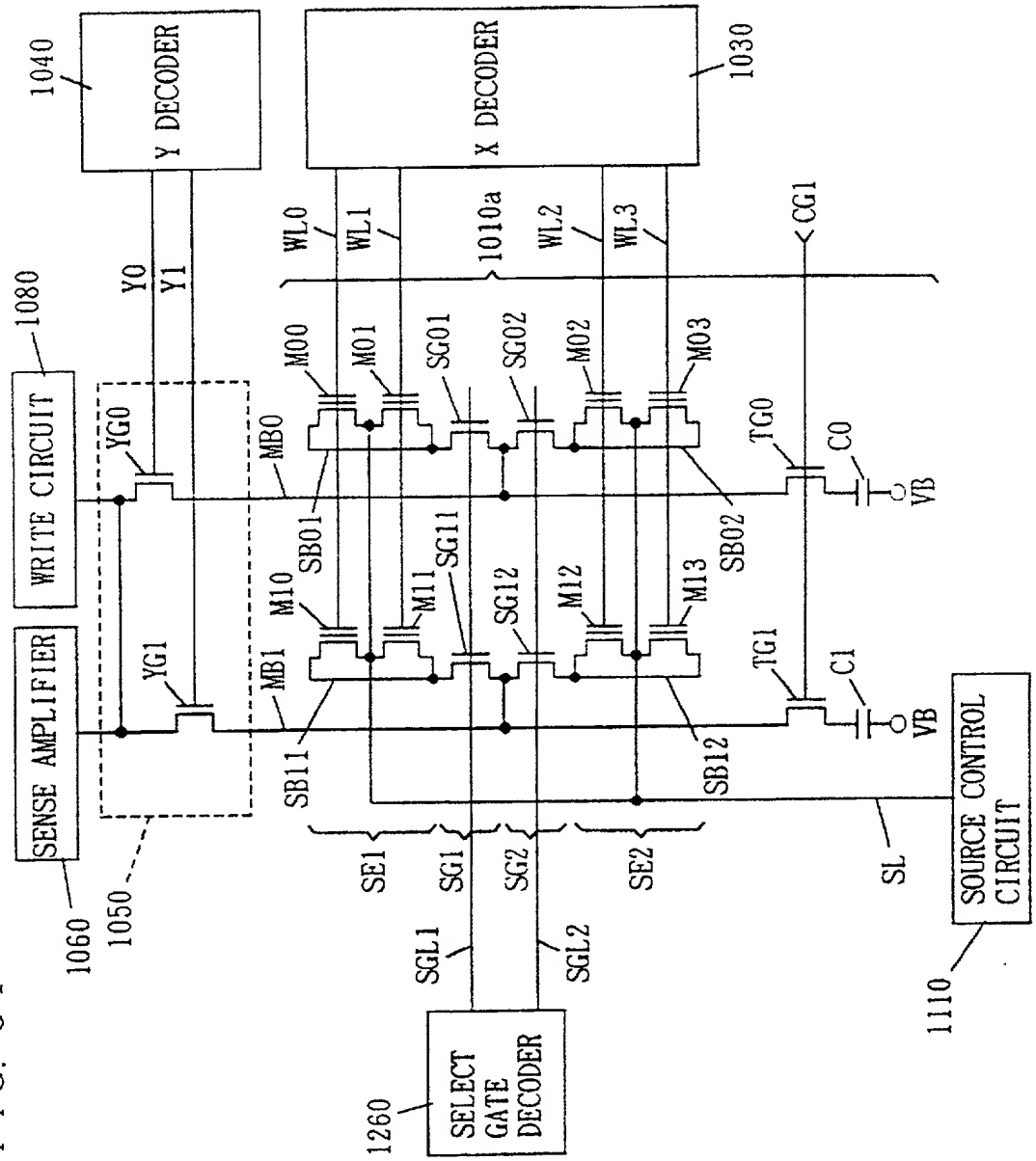

1040
Y DECODER
1030
X DECODER
1080
WRITE CIRCUIT
SENSE AMPLIFIER
1060
1050
1260
SELECT GATE DECODER
1110
SOURCE CONTROL CIRCUIT
Y0
Y1
YG0
YG1
MB0
MB1
WL0
WL1
1010a
WL2
WL3
CG1
M00
M01
SG01
SG02
M02
M03
TG0
C0
VB
SB01
M10
M11
SG11
SG12
M12
M13
SB02
TG1
C1
SB11
SB12
SE1
SG1
SG2
SE2
SL
SGL1
SGL2

FIG. 34

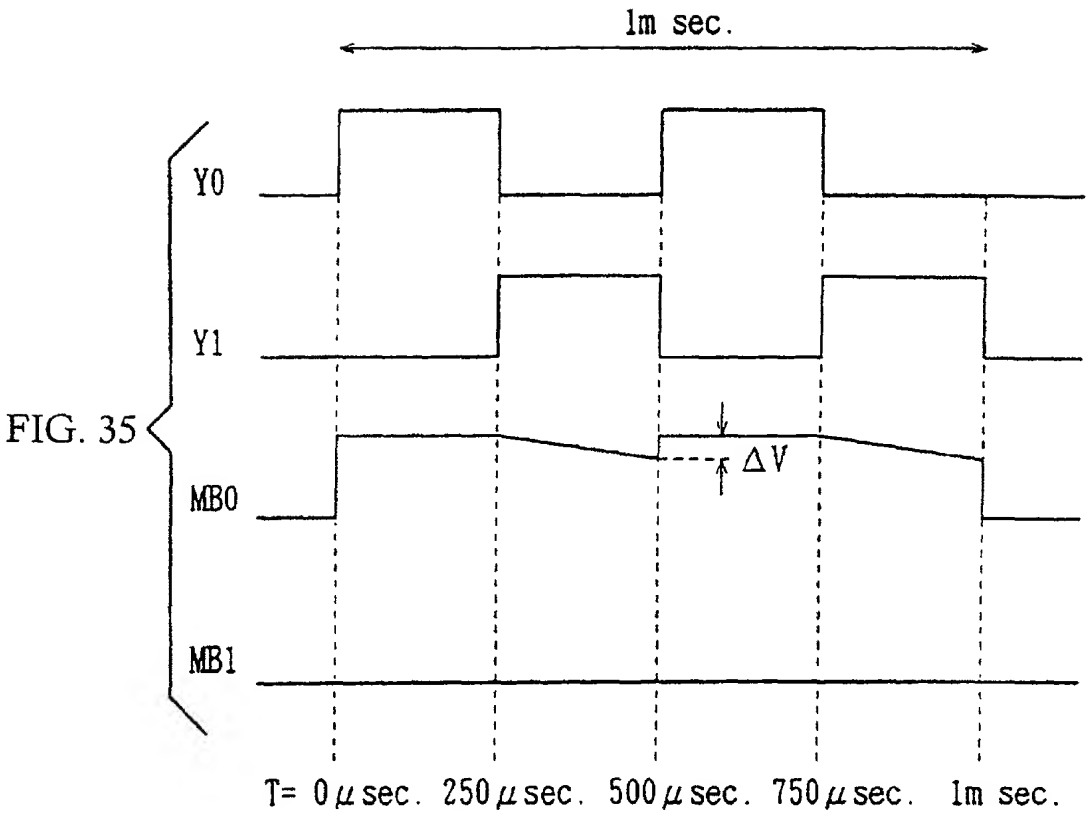


FIG. 35

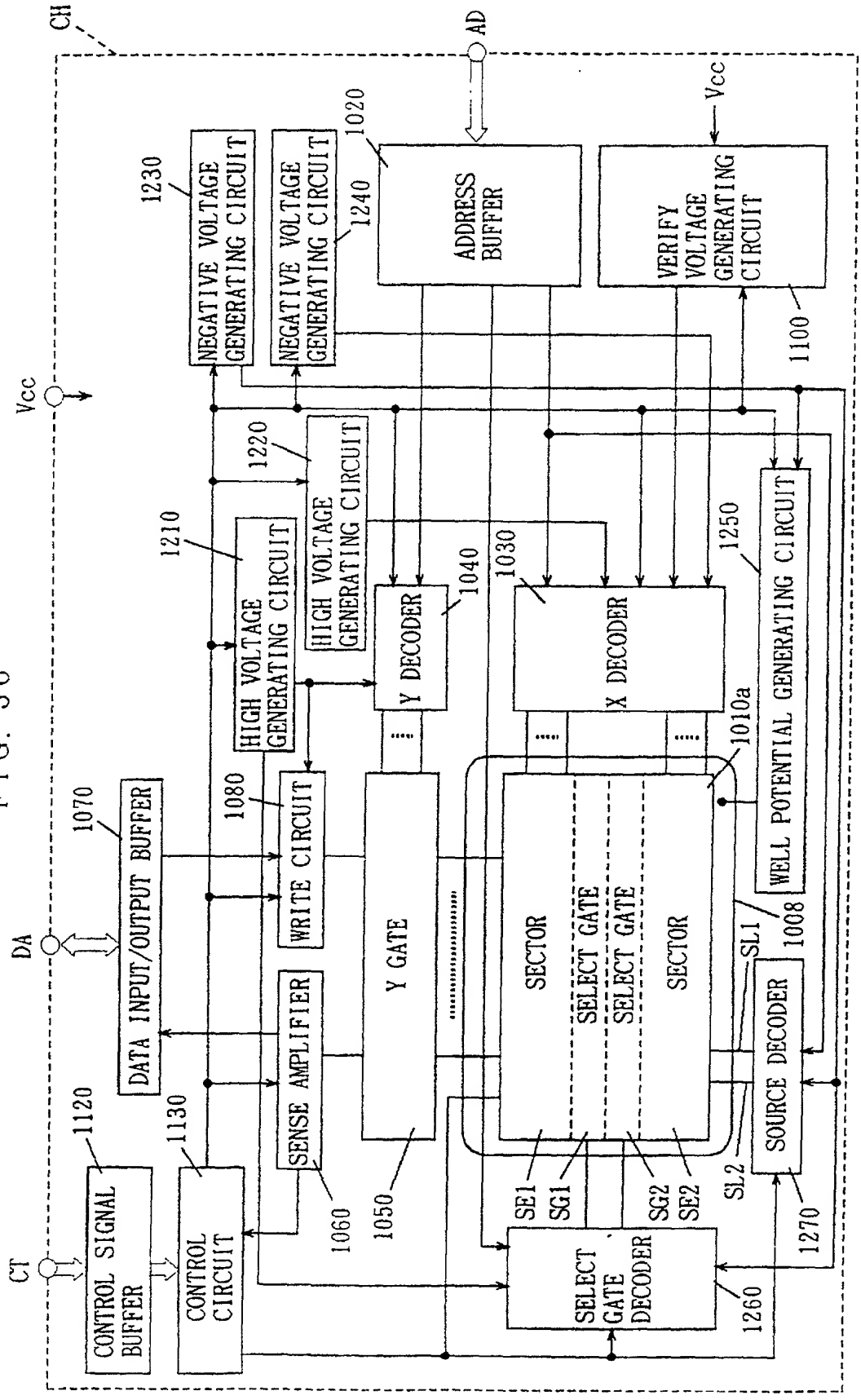

CH
AD
Vcc
Vcc
1230
NEGATIVE VOLTAGE GENERATING CIRCUIT
1020
NEGATIVE VOLTAGE GENERATING CIRCUIT
1240
ADDRESS BUFFER
VERIFY VOLTAGE GENERATING CIRCUIT
1100
1220
HIGH VOLTAGE GENERATING CIRCUIT
1210
HIGH VOLTAGE GENERATING CIRCUIT
1040
Y DECODER
1030
X DECODER
1250
WELL POTENTIAL GENERATING CIRCUIT
1010a
1070
DATA INPUT/OUTPUT BUFFER
1080
WRITE CIRCUIT
Y GATE
SECTOR
SELECT GATE
SELECT GATE
SECTOR
SL1
1008
DA
1120
CONTROL SIGNAL BUFFER
1130
CONTROL CIRCUIT
SENSE AMPLIFIER
1060
1050
SE1
SG1
SG2
SE2
SL2
SOURCE DECODER
1270
CT
SELECT GATE DECODER
1260

FIG. 36

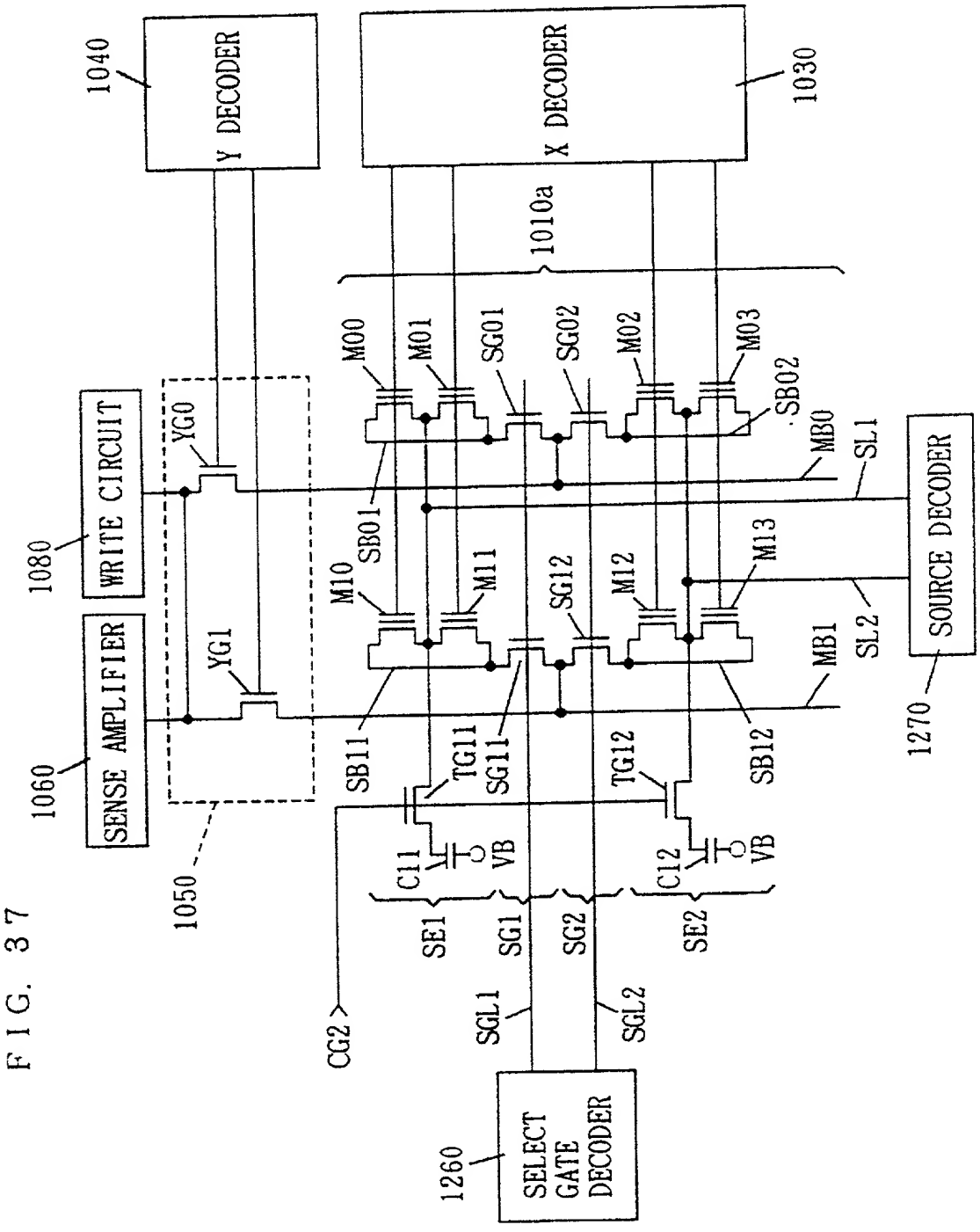

1040
Y DECODER
1030
X DECODER
1010a
M00
M01
SG01
SG02
M02
M03
SB02
MB0
SL1
SOURCE DECODER
1270
1080
WRITE CIRCUIT
YG0
SB01
M10
M11
SG12
M12
M13
SL2
MB1
1060
SENSE AMPLIFIER
YG1
SB11
TG11
SG11
TG12
SB12
1050
C11
VB
C12
VB
SE1
SG1
SG2
SE2
CG2
SGL1
SGL2
1260
SELECT GATE DECODER

FIG. 37

FIG. 38

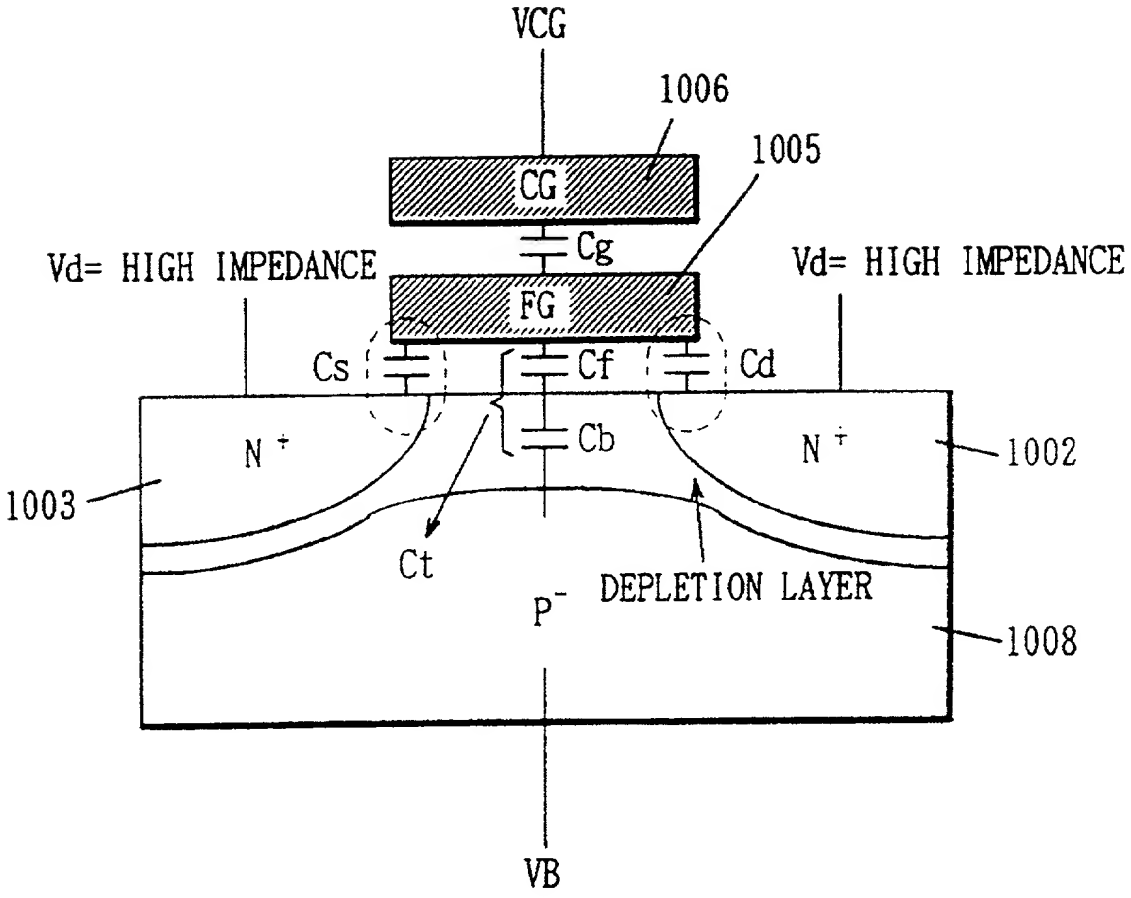

VCG
1006
1005
CG
Cg
Vd= HIGH IMPEDANCE
Vd= HIGH IMPEDANCE
FG
Cs
Cf
Cd
Cb
N +
N +
1003
1002
Ct
P-
DEPLETION LAYER
1008
VB

FIG. 39A

[ERASING WITH NO GATE BIRD'S BEAK]

(MEMORY CELL OF SELECTED SECTOR)

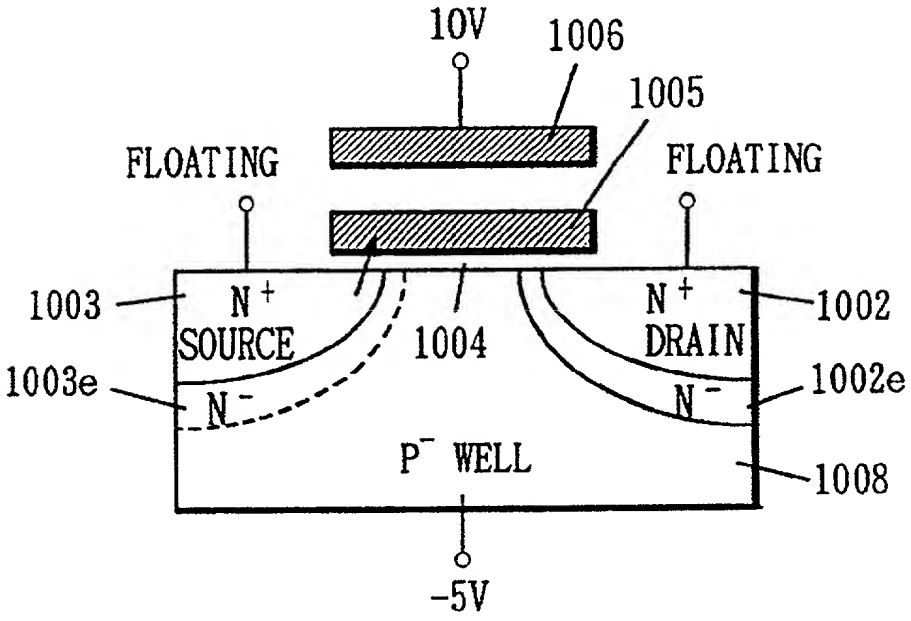


FIG. 39B

(MEMORY CELL OF NONSELECTED SECTOR)

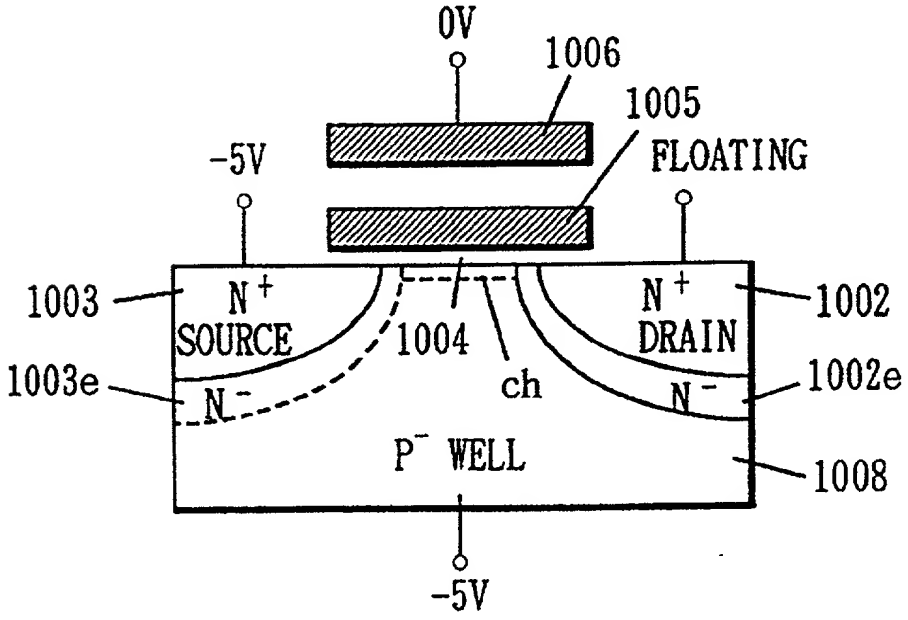


FIG. 40

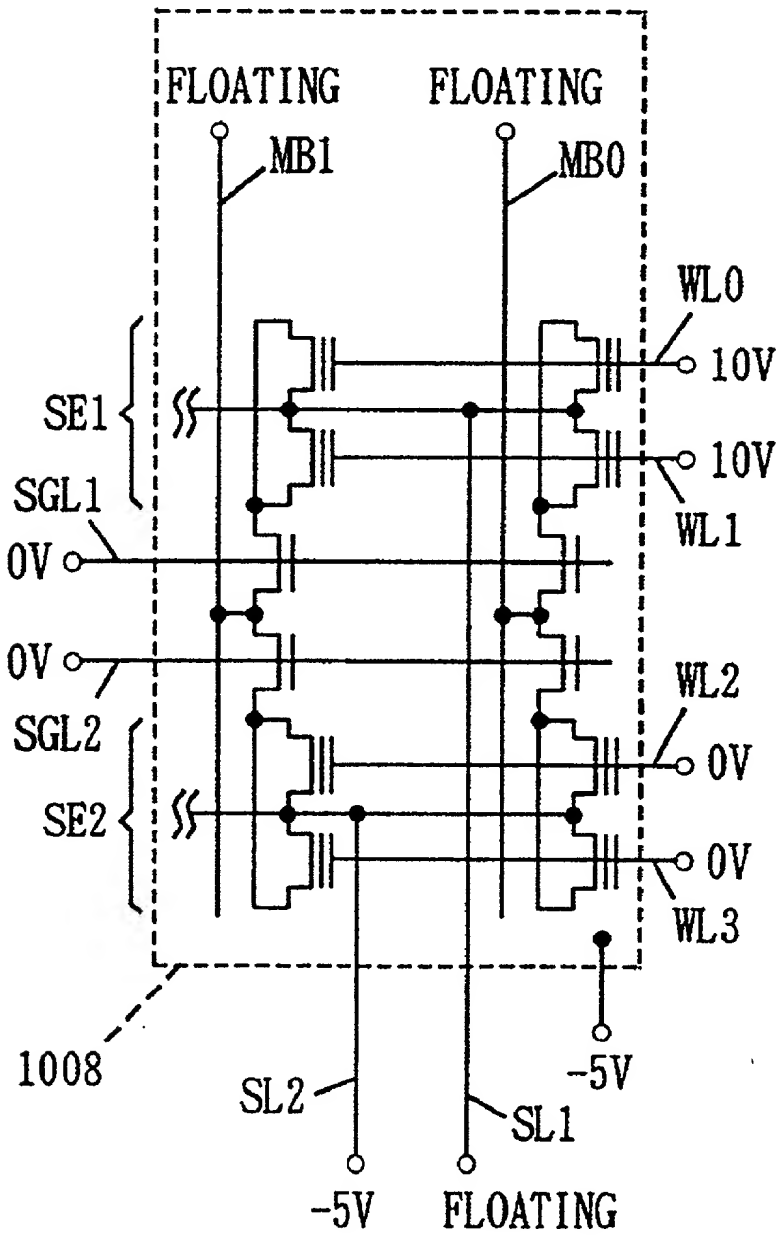
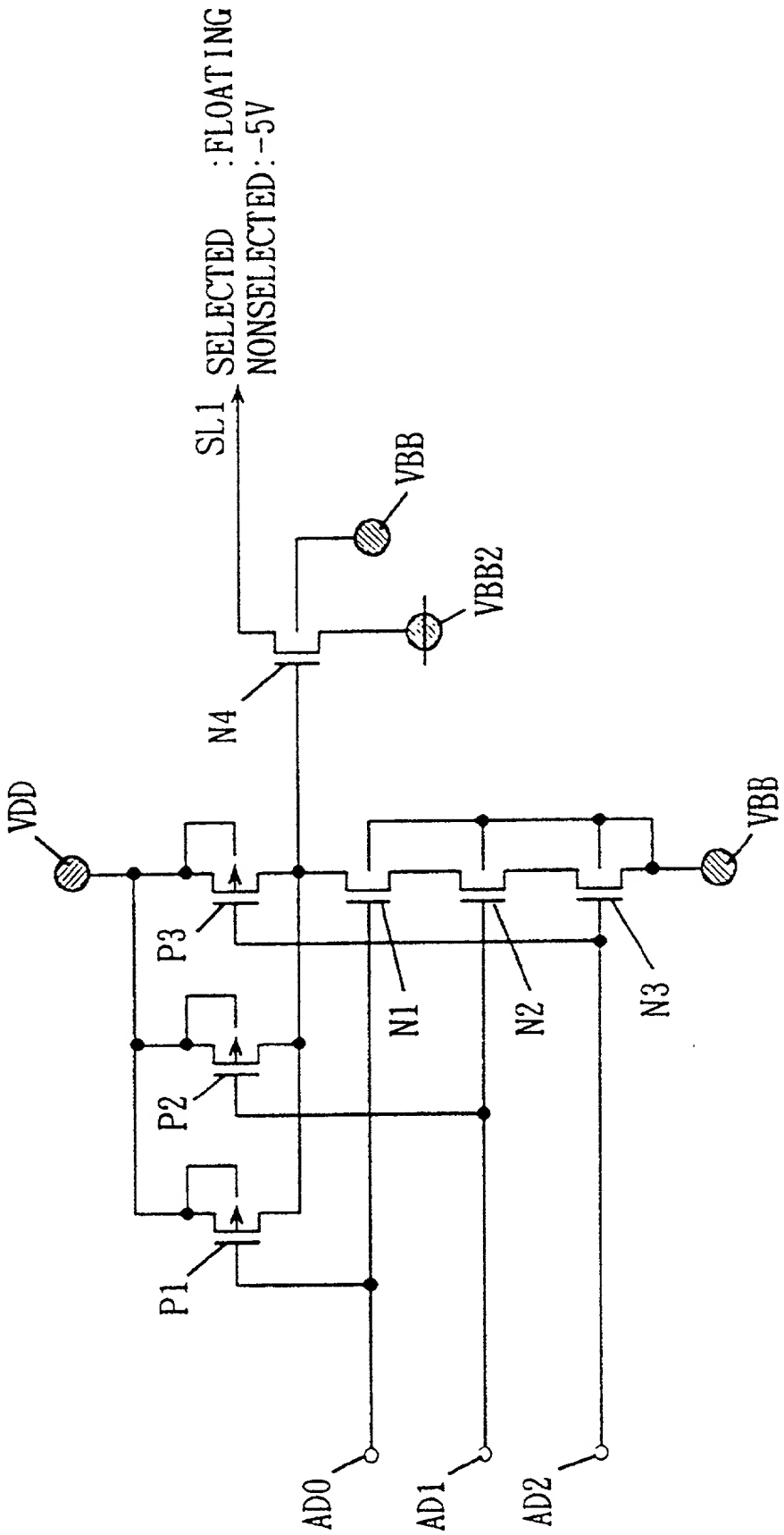

[WITH NO GATE BIRD'S BEAK]
(BATCH SECTOR ERASE)
FLOATING
FLOATING
MB1
MB0
WL0
10V
SE1
10V
SGL1
WL1
0V
0V
WL2
SGL2
0V
SE2
0V
WL3
1008
-5V
SL2
SL1
-5V
FLOATING

FIG. 41


SL1 SELECTED :FLOATING
NONSELECTED:-5V
VBB
VBB2
N4
VDD
VBB
P3
P2
P1
N1
N2
N3
AD0
AD1
AD2

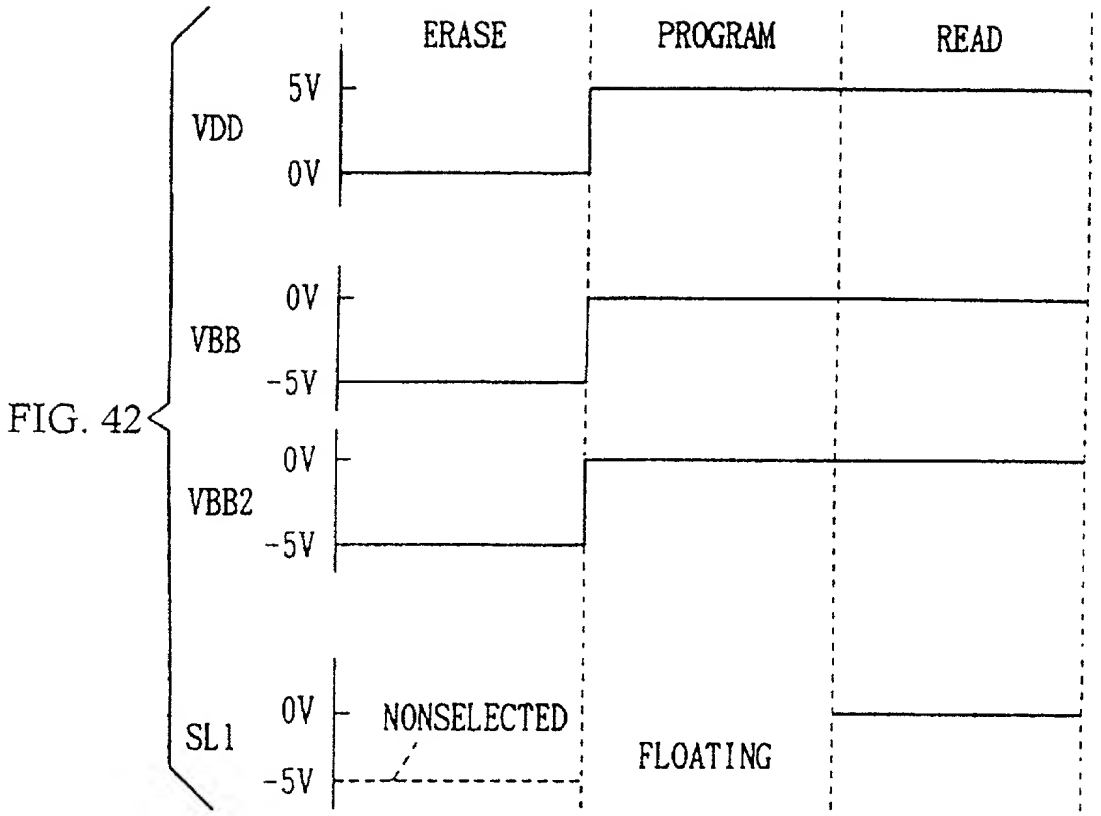

ERASE
PROGRAM
READ
VDD
5V
0V
VBB
0V
-5V
VBB2
0V
-5V
SL1
0V
-5V
NONSELECTED
FLOATING

FIG. 42

FIG. 43

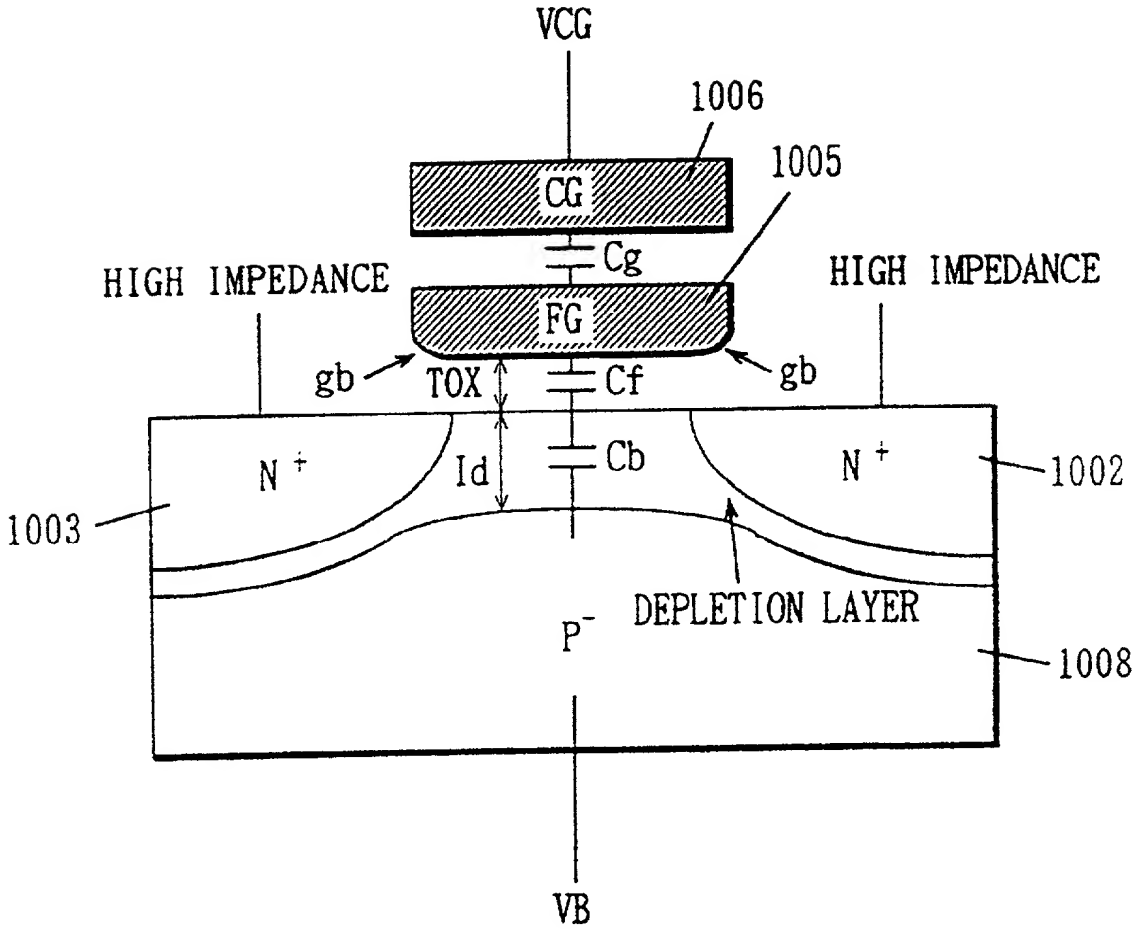

VCG
1006
1005
CG
Cg
HIGH IMPEDANCE
HIGH IMPEDANCE
FG
gb
TOX
Cf
gb
N +
Id
Cb
N +
1002
1003
DEPLETION LAYER
P-
1008
VB

FIG. 44A

[ERASING WITH GATE BIRD'S BEAK]

(MEMORY CELL OF SELECTED SECTOR)

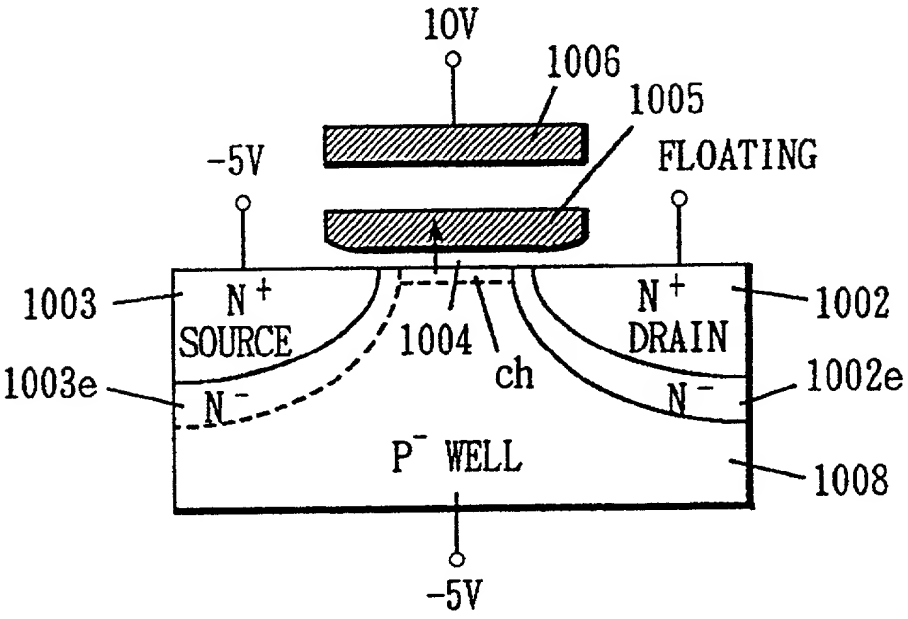


FIG. 44B

(MEMORY CELL OF NONSELECTED SECTOR)

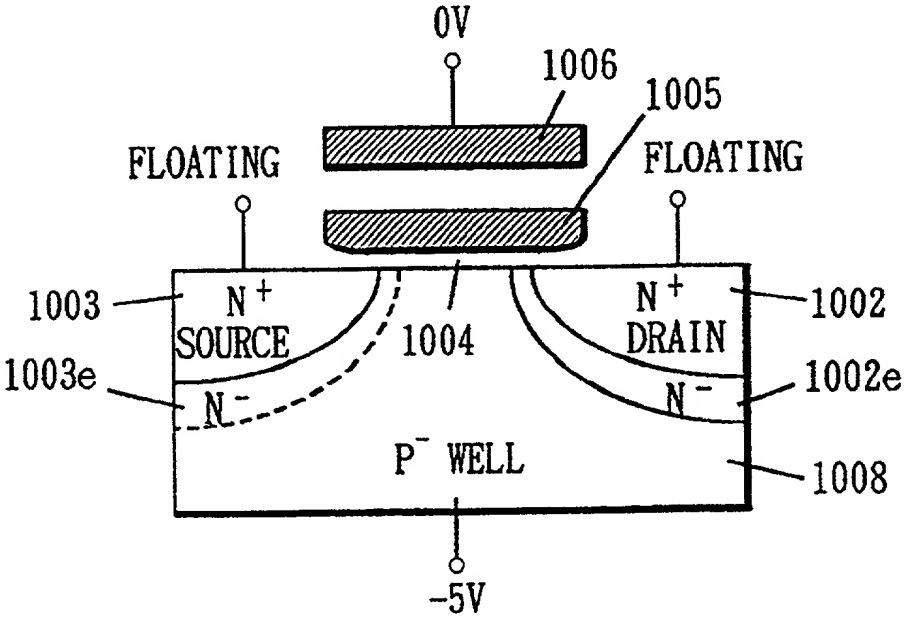


FIG. 45

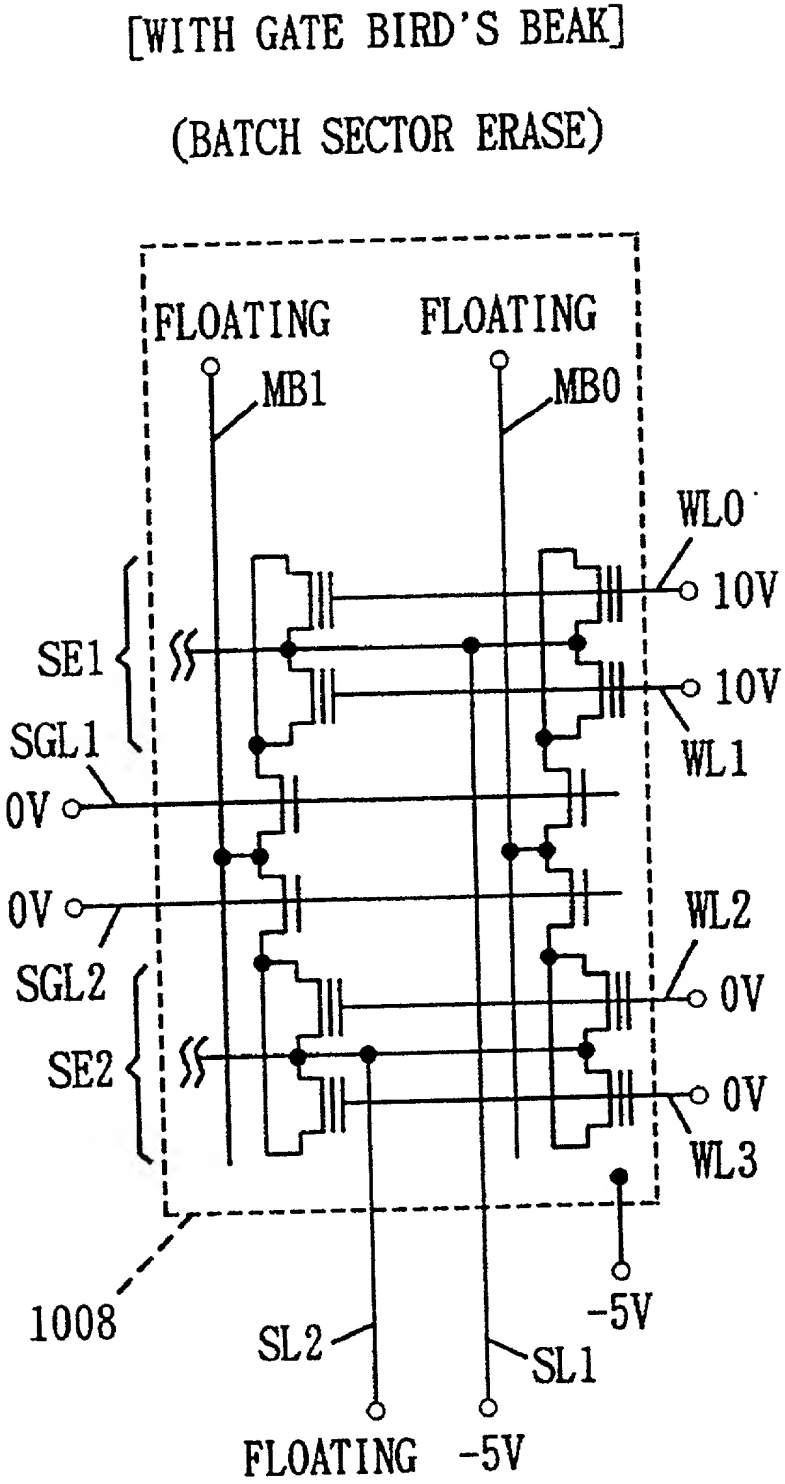
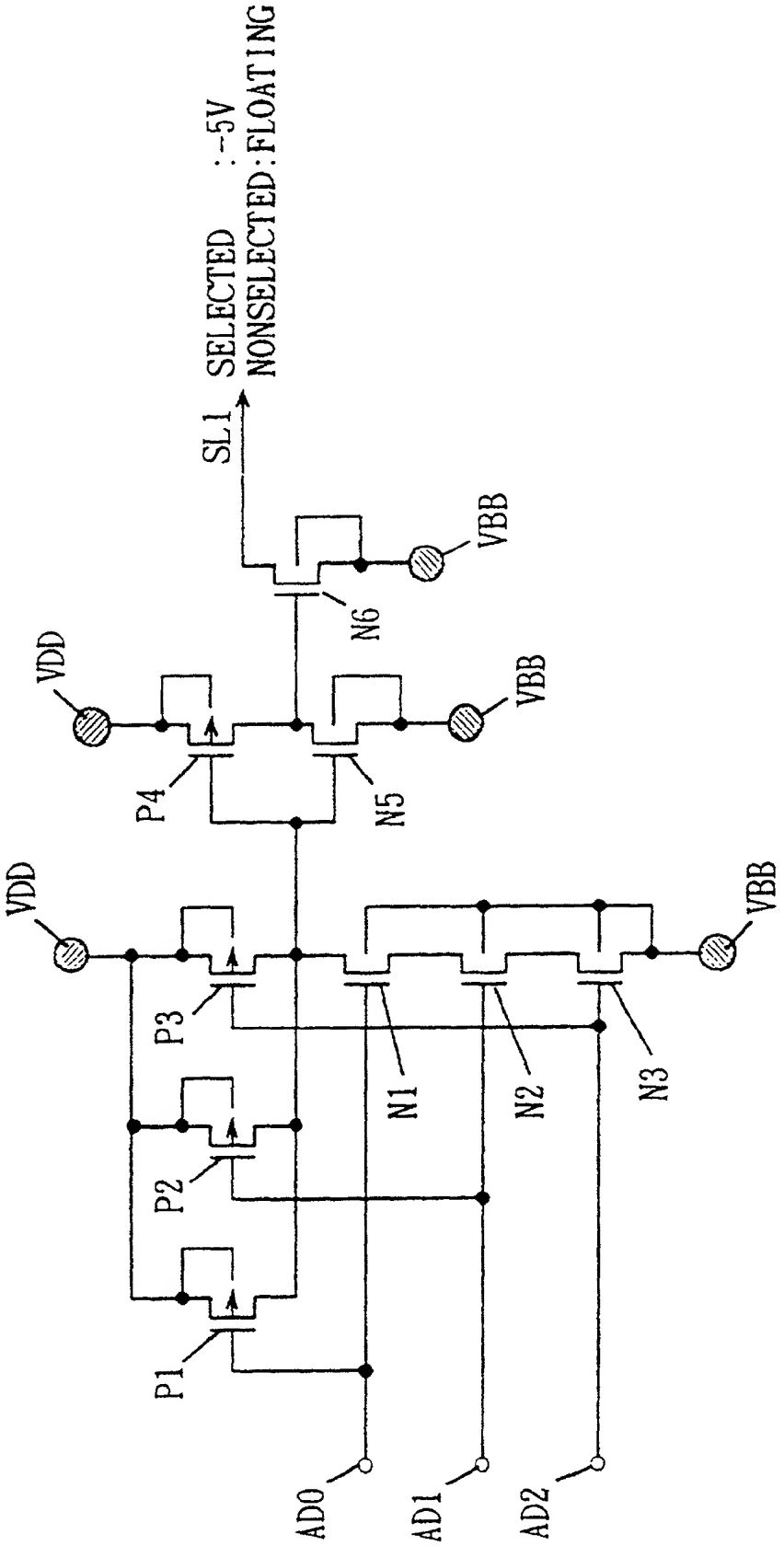

[WITH GATE BIRD'S BEAK]
(BATCH SECTOR ERASE)
FLOATING
FLOATING
MB1
MB0
WL0
10V
SE1
10V
SGL1
WL1
0V
0V
WL2
SGL2
0V
SE2
0V
WL3
1008
-5V
SL2
SL1
FLOATING
-5V

FIG. 46


SL1
SELECTED :-5V
NONSELECTED:FLOATING
VDD
VBB
P1
P2
P3
P4
N1
N2
N3
N5
N6
AD0
AD1
AD2

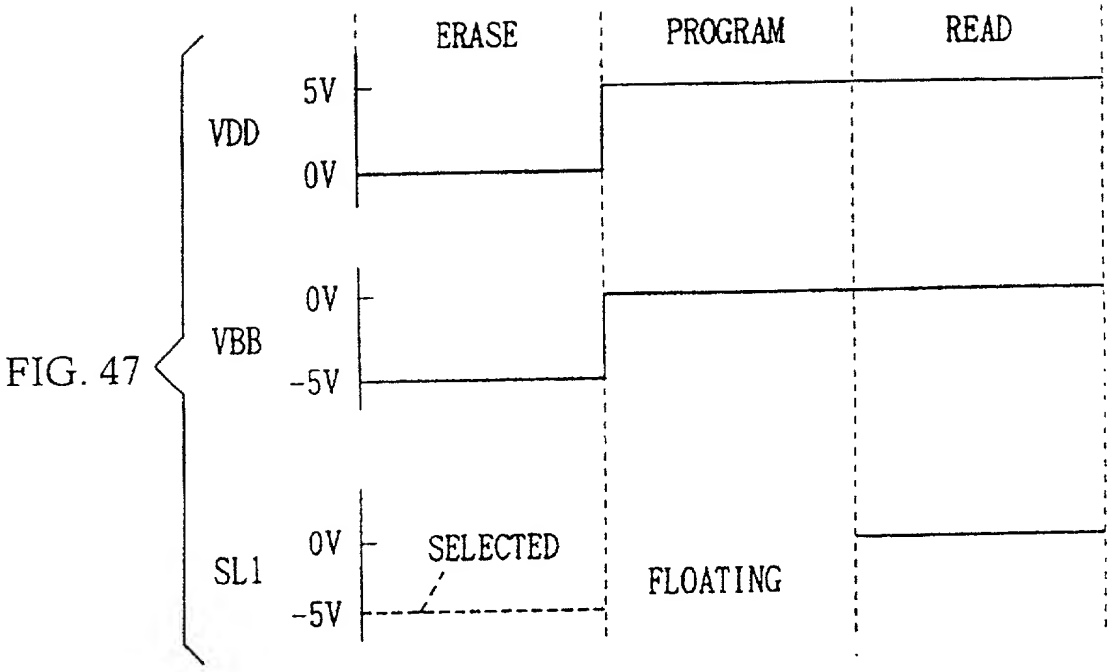

ERASE
PROGRAM
READ
VDD
5V
0V
VBB
0V
-5V
SL1
0V
SELECTED
-5V
FLOATING

FIG. 47

FIG. 48A

[ERASING WITH LOW WELL POTENTIAL]

(MEMORY CELL OF SELECTED SECTOR)

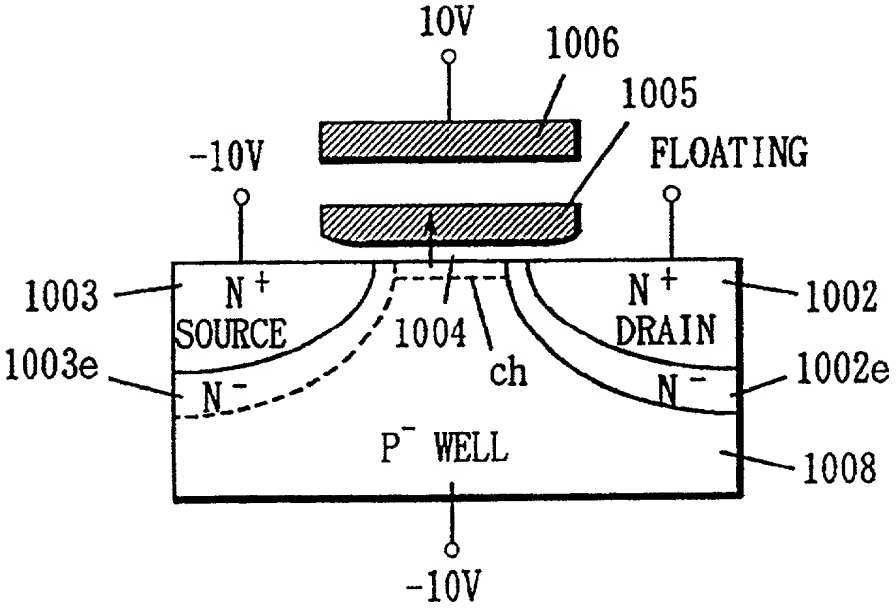


FIG. 48B

(MEMORY CELL OF NONSELECTED SECTOR)

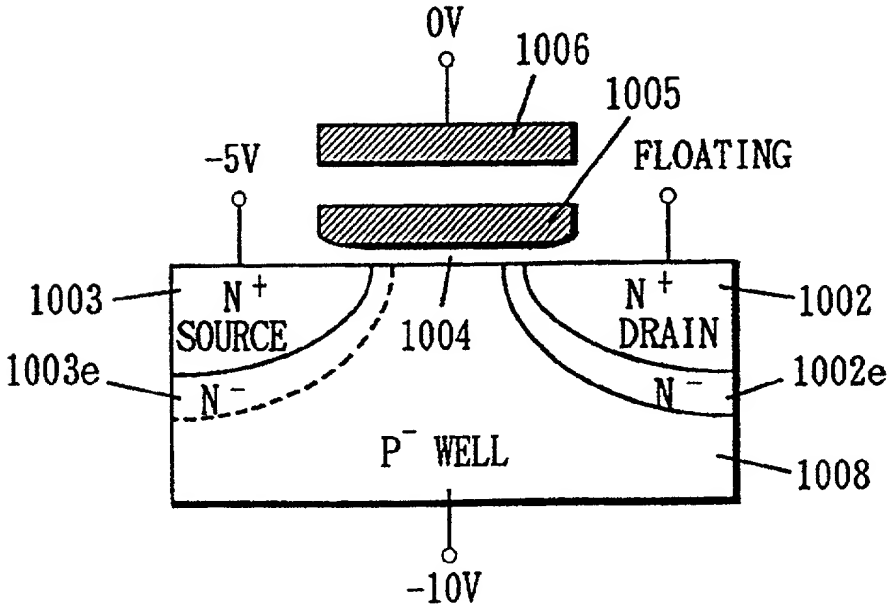


FIG. 49

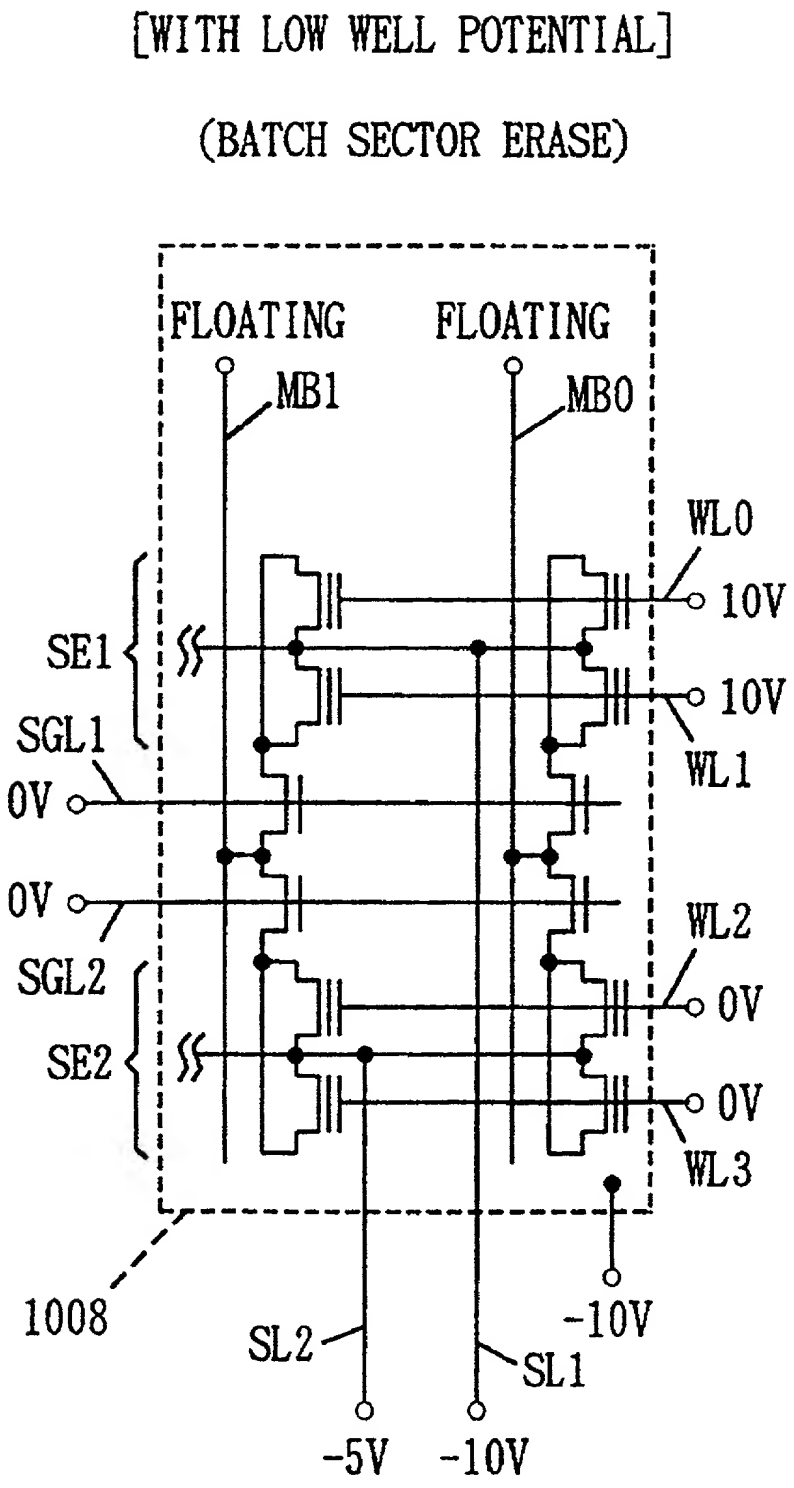
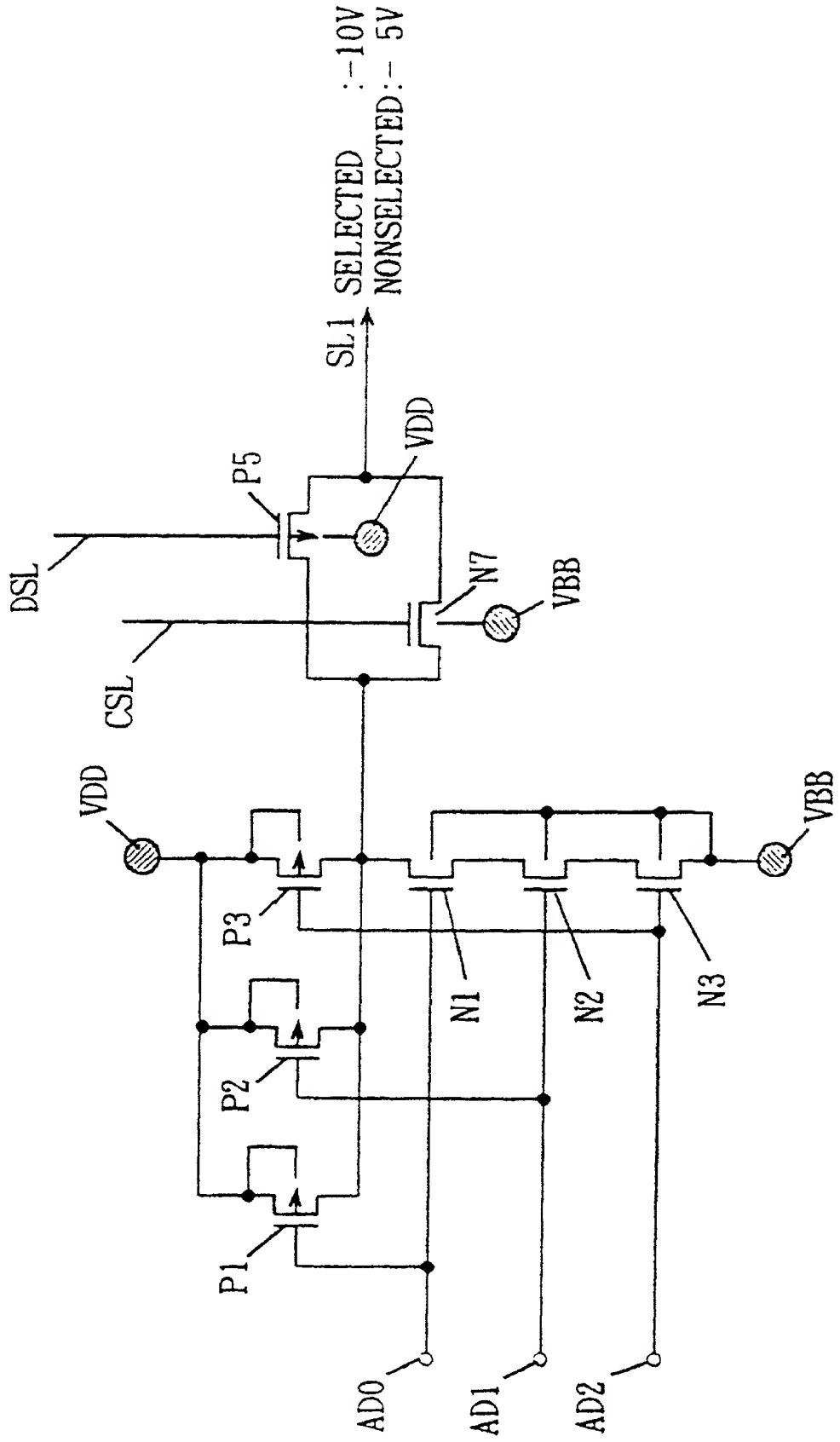

[WITH LOW WELL POTENTIAL]
(BATCH SECTOR ERASE)
FLOATING
FLOATING
MB1
MB0
WL0
10V
SE1
10V
SGL1
WL1
0V
0V
WL2
SGL2
0V
SE2
0V
WL3
1008
SL2
SL1
-10V
-5V
-10V

FIG. 50


SL1 SELECTED :-10V
NONSELECTED:- 5V
VDD
P5
DSL
N7
VBB
CSL
VDD
VBB
P3
N1
N2
N3
P2
P1
AD0
AD1
AD2

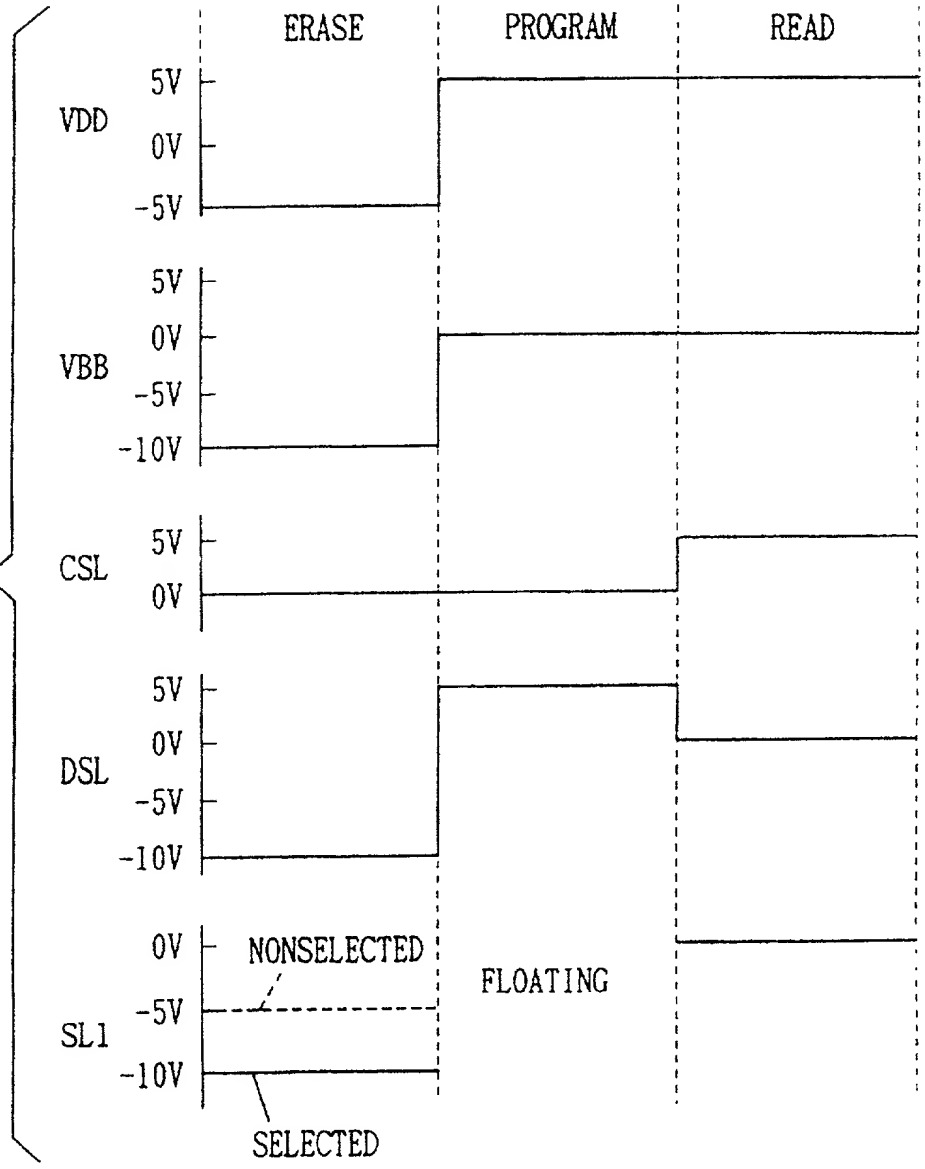


FIG. 51

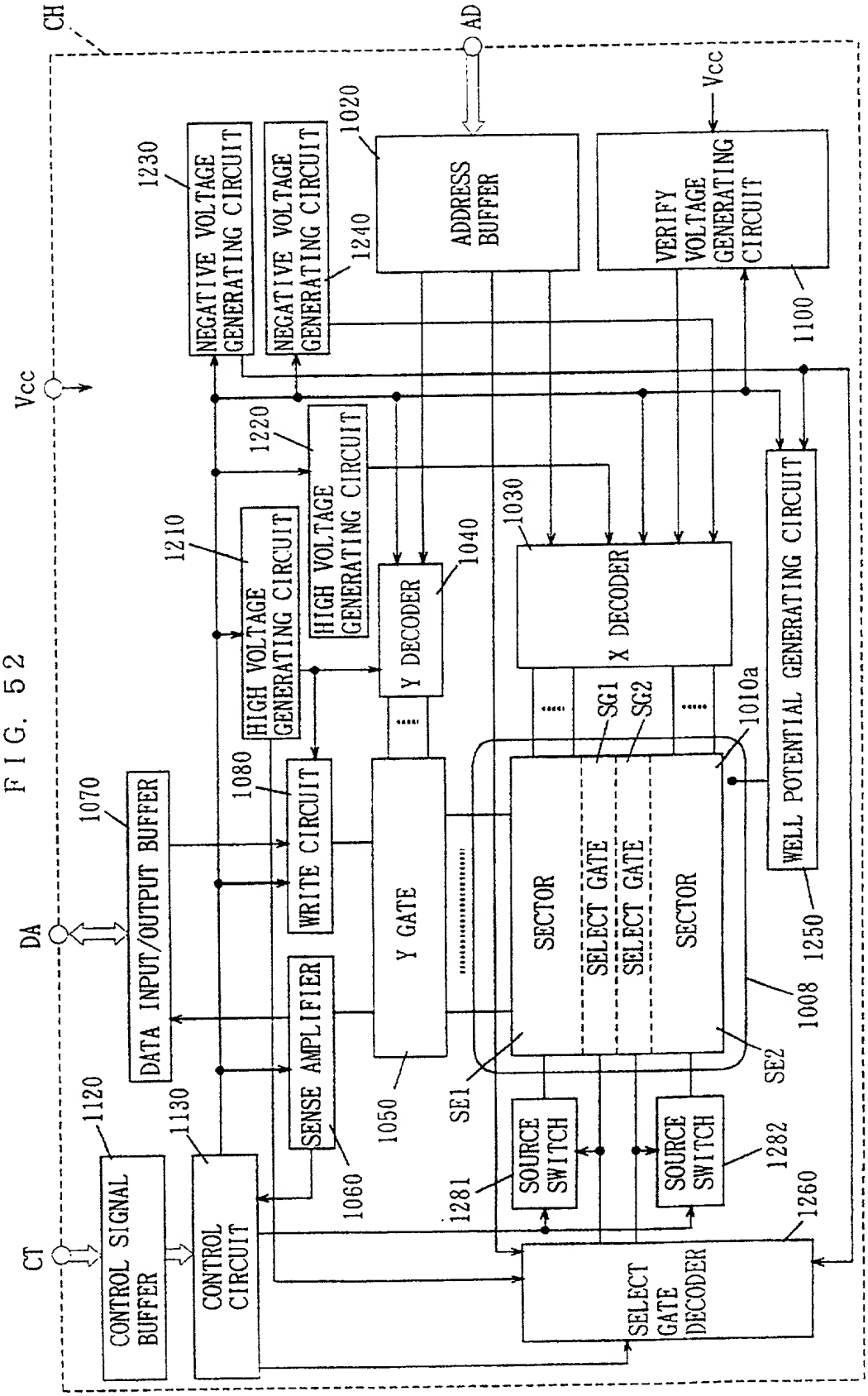

CH
AD
Vcc
Vcc
NEGATIVE VOLTAGE GENERATING CIRCUIT
1230
NEGATIVE VOLTAGE GENERATING CIRCUIT
1240
1020
ADDRESS BUFFER
VERIFY VOLTAGE GENERATING CIRCUIT
1100
1220
HIGH VOLTAGE GENERATING CIRCUIT
1210
HIGH VOLTAGE GENERATING CIRCUIT
Y DECODER
1040
1030
X DECODER
WELL POTENTIAL GENERATING CIRCUIT
1250
1070
DATA INPUT/OUTPUT BUFFER
1080
WRITE CIRCUIT
Y GATE
SECTOR
SELECT GATE
SELECT GATE
SECTOR
SG1
SG2
1010a
1008
SE2
SE1
1050
DA
1120
CONTROL SIGNAL BUFFER
1130
CONTROL CIRCUIT
SENSE AMPLIFIER
1060
1281
SOURCE SWITCH
SOURCE SWITCH
1282
1260
SELECT GATE DECODER
CT

FIG. 52

FIG. 53

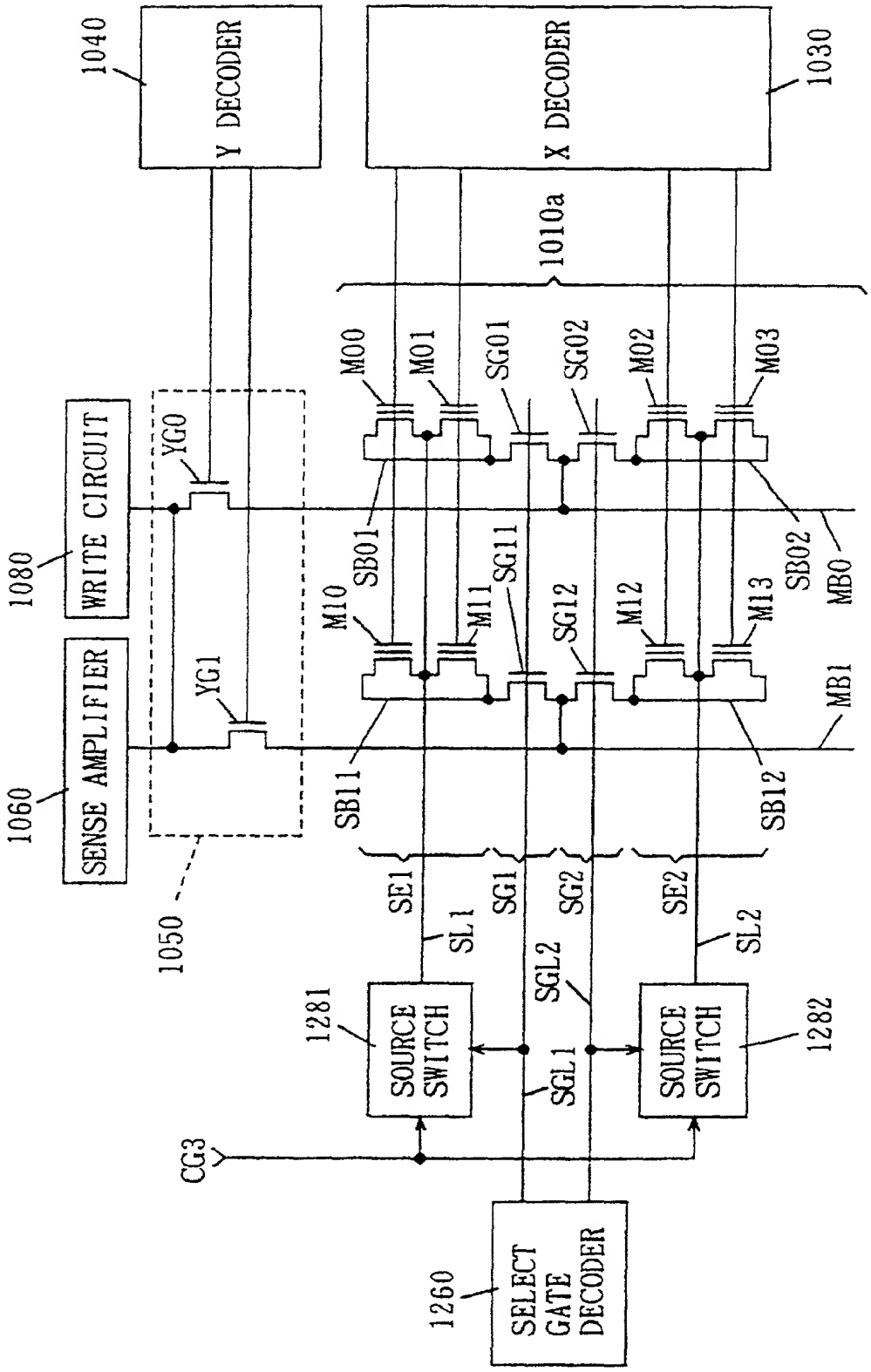

1040
Y DECODER
1030
X DECODER
1010a
M00
M01
SG01
SG02
M02
M03
YG0
1080
WRITE CIRCUIT
SB01
M10
M11
SG11
SG12
M12
M13
SB02
MB0
YG1
1060
SENSE AMPLIFIER
SB11
SB12
MB1
1050
SE1
SL1
SG1
SG2
SE2
SL2
SGL2
1281
SOURCE SWITCH
SGL1
SOURCE SWITCH
1282
CG3
1260
SELECT GATE DECODER

FIG. 54

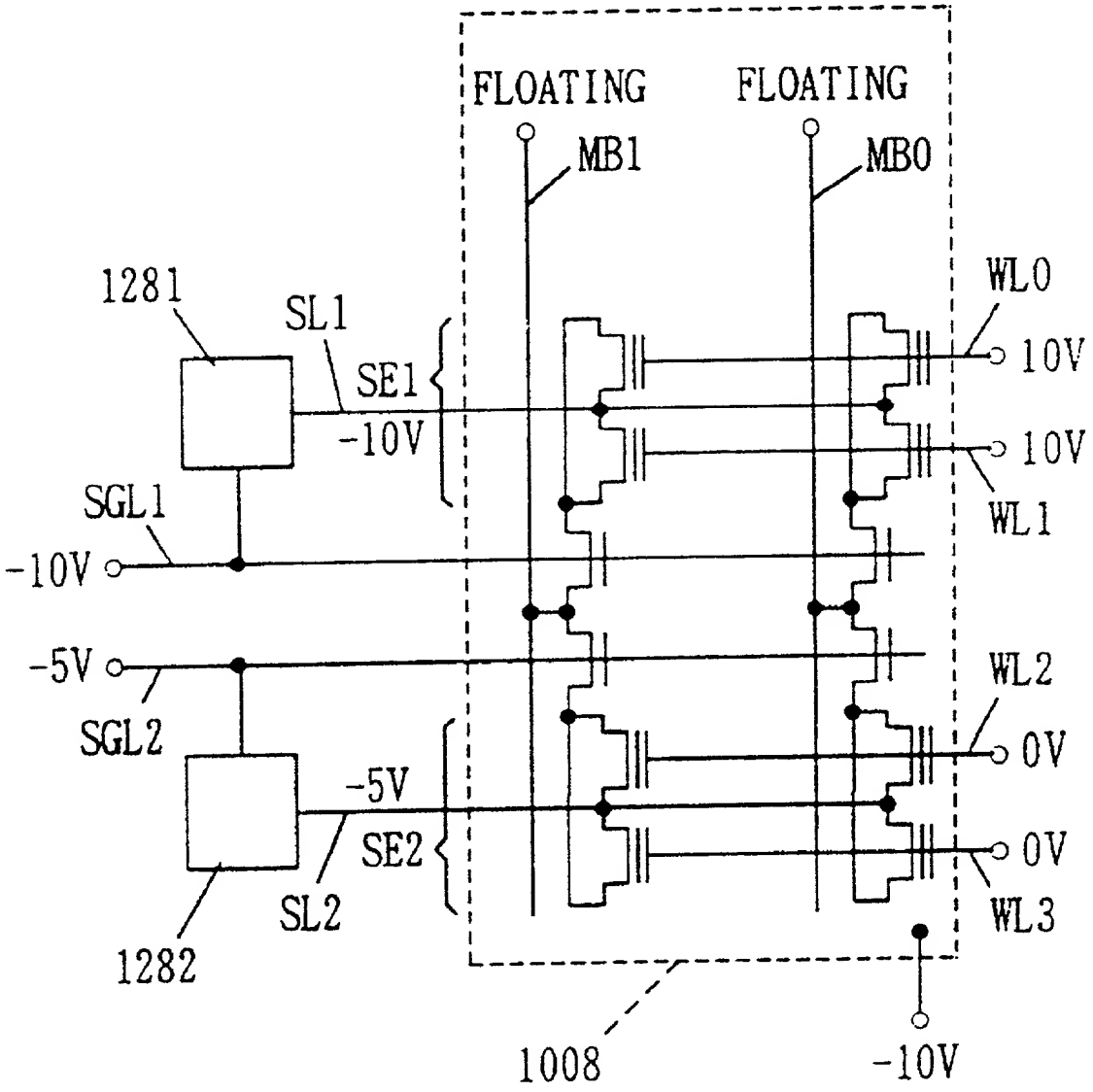
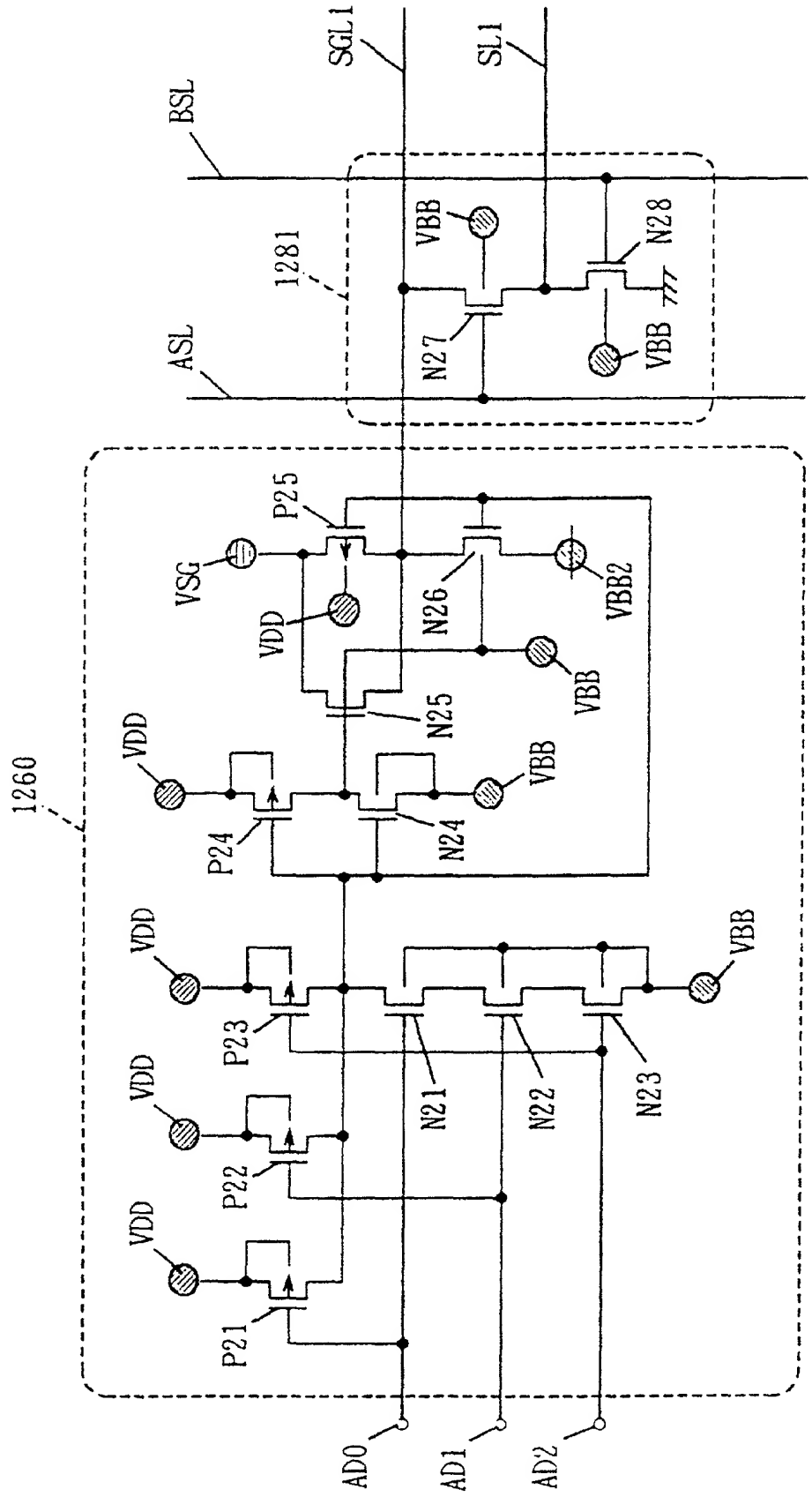

FLOATING
FLOATING
MB1
MB0
1281
SL1
SE1
-10V
WL0
10V
10V
WL1
SGL1
-10V
-5V
WL2
SGL2
0V
-5V
SE2
0V
WL3
SL2
1282
1008
-10V

FIG. 55


SGL1
SL1
BSL
ASL
1281
VBB
N28
N27
VBB
1260
P25
VSG
VDD
N26
VBB2
VBB
N25
VDD
VBB
P24
N24
VDD
VBB
P23
N21
N22
N23
VDD
P22
VDD
P21
AD0
AD1
AD2

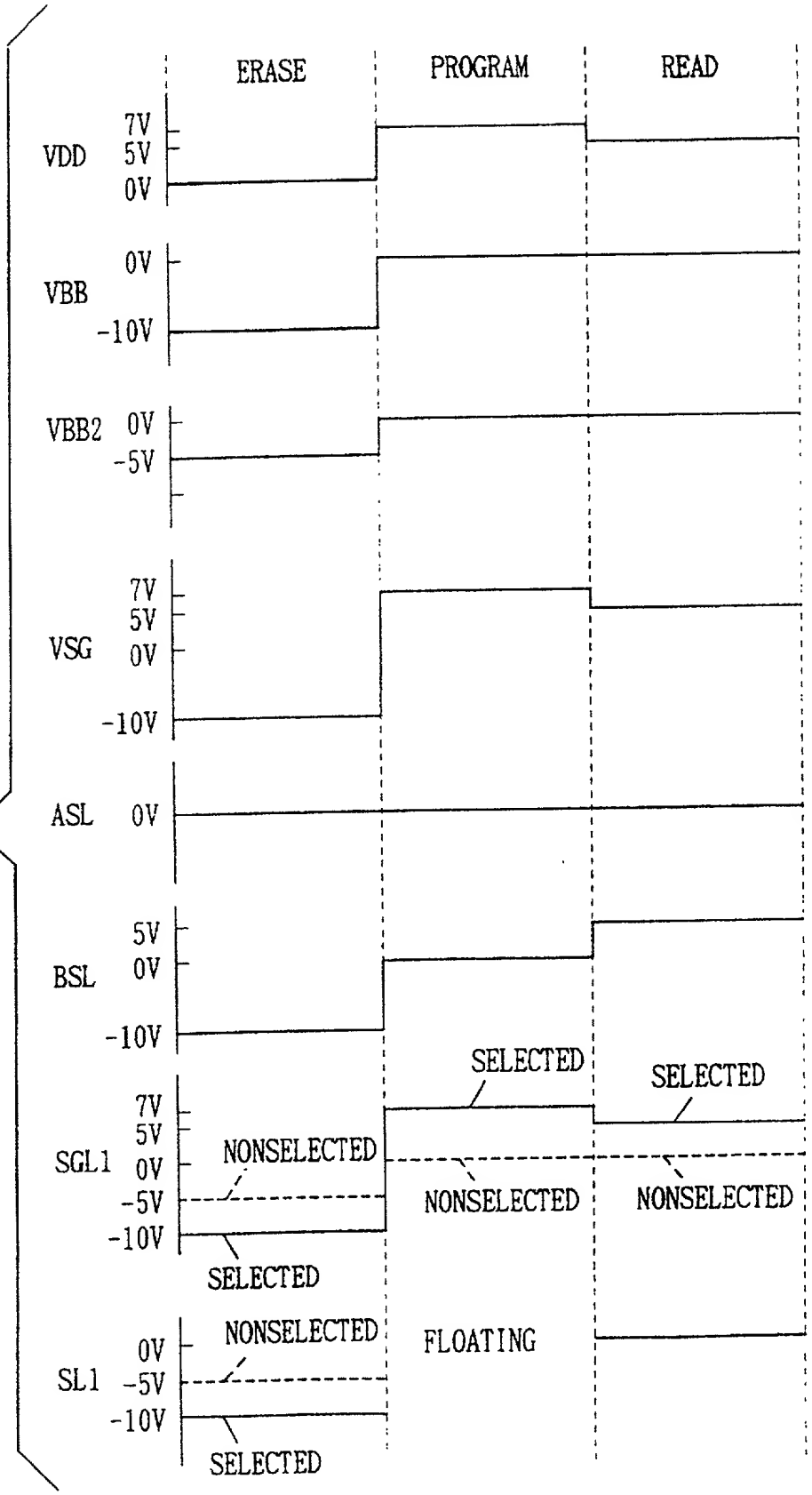

ERASE
PROGRAM
READ
VDD
7V
5V
0V
VBB
0V
-10V
VBB2
0V
-5V
VSG
7V
5V
0V
-10V
ASL
0V
BSL
5V
0V
-10V
SGL1
7V
5V
0V
-5V
-10V
NONSELECTED
SELECTED
SELECTED
NONSELECTED
NONSELECTED
SELECTED
SL1
0V
-5V
-10V
NONSELECTED
FLOATING
SELECTED

FIG. 56

FIG. 57

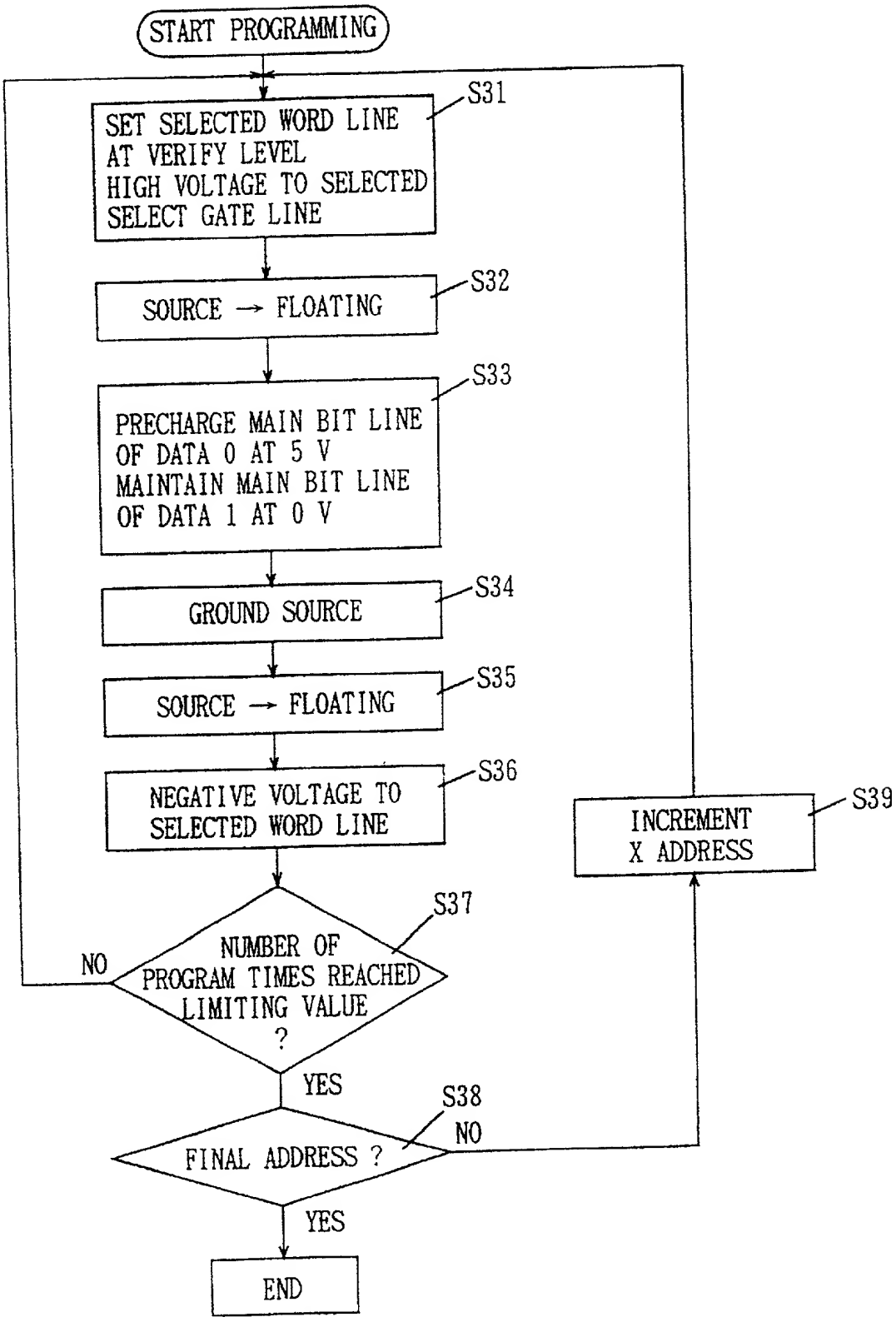
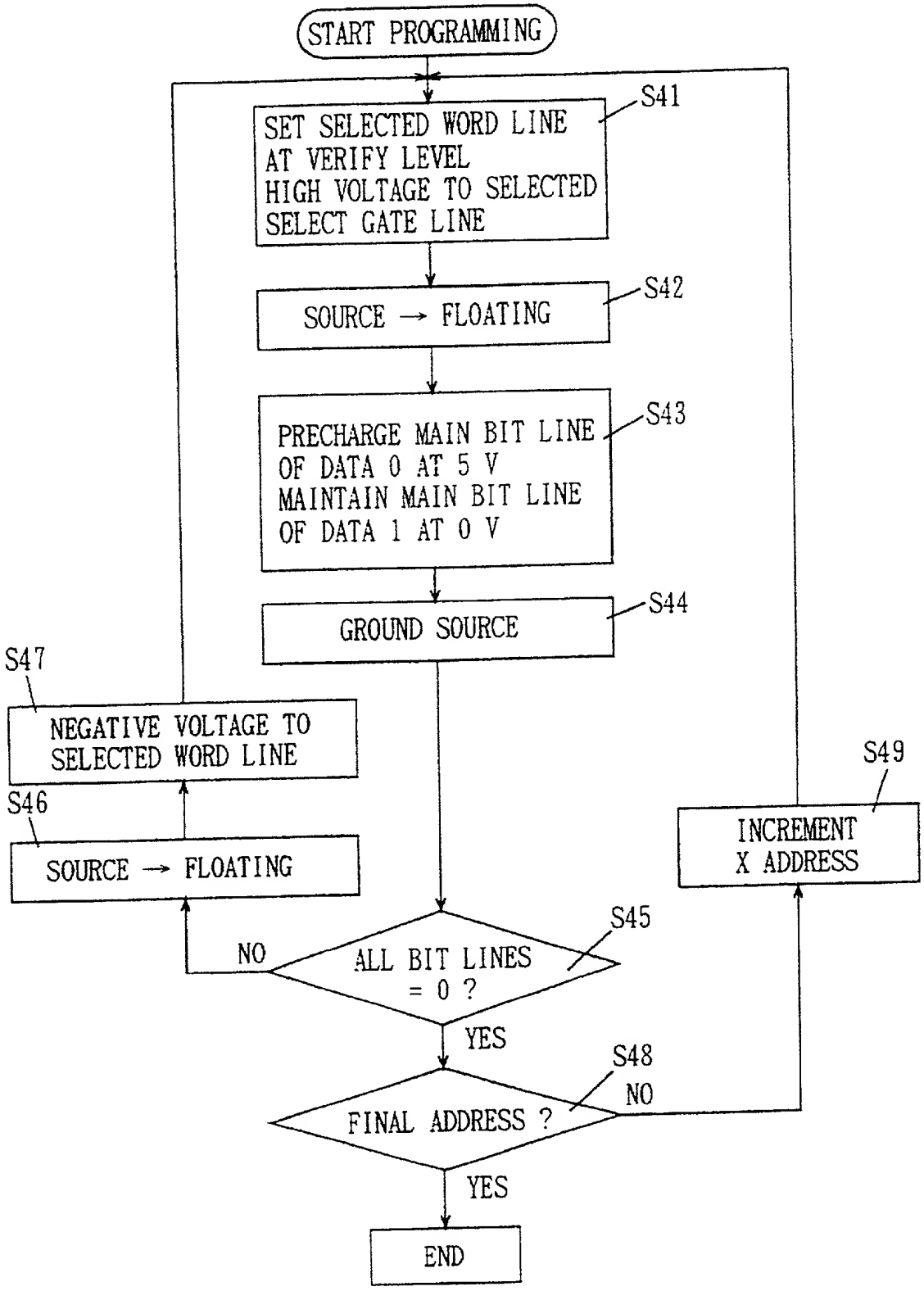

START PROGRAMMING
S31
SET SELECTED WORD LINE AT VERIFY LEVEL HIGH VOLTAGE TO SELECTED SELECT GATE LINE
S32
SOURCE → FLOATING
S33
PRECHARGE MAIN BIT LINE OF DATA 0 AT 5 V MAINTAIN MAIN BIT LINE OF DATA 1 AT 0 V
S34
GROUND SOURCE
S35
SOURCE → FLOATING
S36
NEGATIVE VOLTAGE TO SELECTED WORD LINE
S37
NUMBER OF PROGRAM TIMES REACHED LIMITING VALUE ?
NO
YES
S38
FINAL ADDRESS ?
NO
YES
S39
INCREMENT X ADDRESS
END

FIG. 58


START PROGRAMMING
S41
SET SELECTED WORD LINE AT VERIFY LEVEL HIGH VOLTAGE TO SELECTED SELECT GATE LINE
S42
SOURCE → FLOATING
S43
PRECHARGE MAIN BIT LINE OF DATA 0 AT 5 V MAINTAIN MAIN BIT LINE OF DATA 1 AT 0 V
S44
GROUND SOURCE
S47
NEGATIVE VOLTAGE TO SELECTED WORD LINE
S46
SOURCE → FLOATING
S49
INCREMENT X ADDRESS
S45
ALL BIT LINES = 0 ?
NO
YES
S48
FINAL ADDRESS ?
NO
YES
END

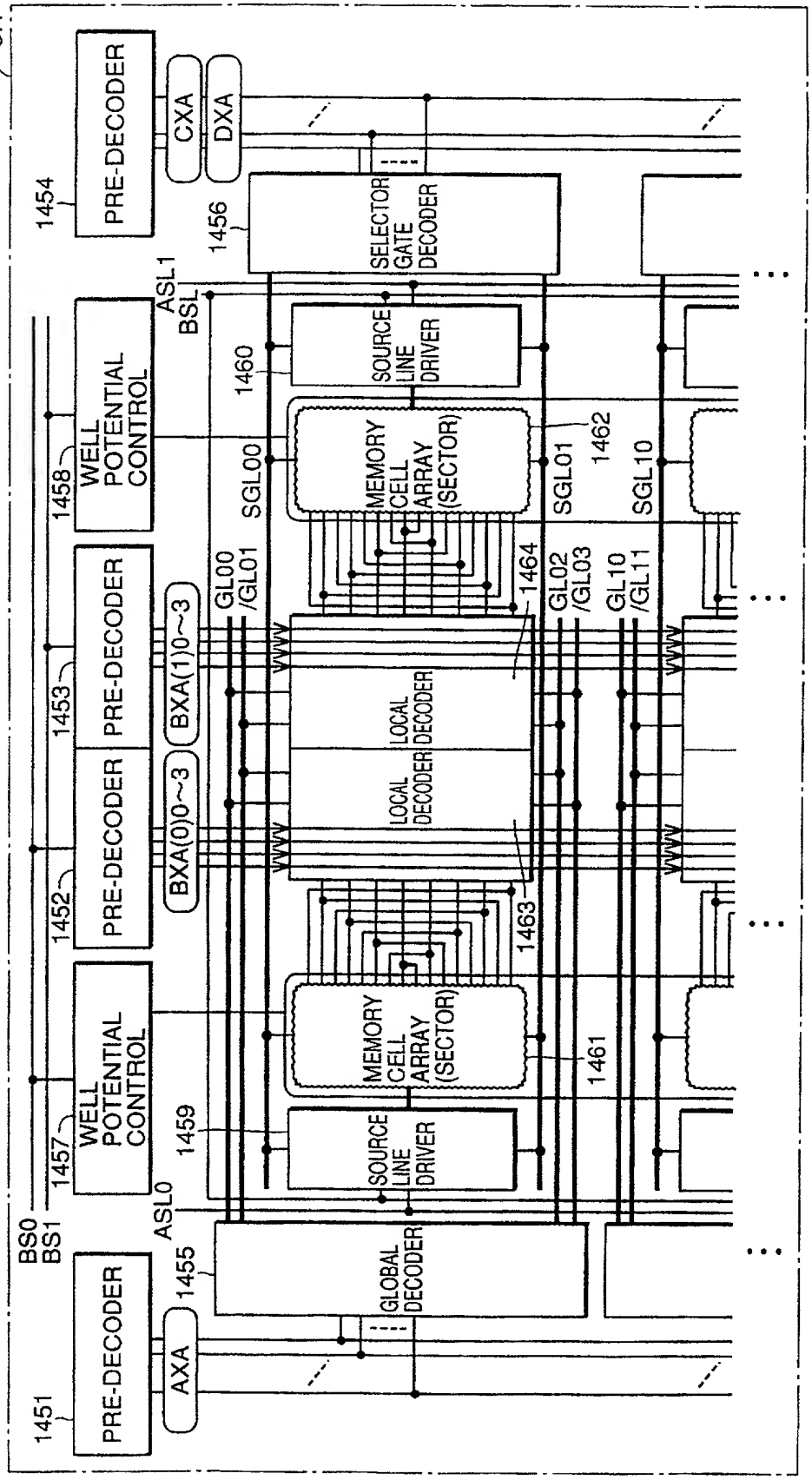

CH
PRE-DECODER
1454
CXA
DXA
SELECTOR GATE DECODER
1456
ASL1
BSL
SOURCE LINE DRIVER
1460
WELL POTENTIAL CONTROL
1458
MEMORY CELL ARRAY (SECTOR)
1462
SGL00
SGL01
SGL10
PRE-DECODER
1453
BXA(1)0~3
GL00 /GL01
GL02 /GL03
GL10 /GL11
LOCAL DECODER
1464
PRE-DECODER
1452
BXA(0)0~3
LOCAL DECODER
1463
WELL POTENTIAL CONTROL
1457
MEMORY CELL ARRAY (SECTOR)
1461
SOURCE LINE DRIVER
1459
BS0
BS1
ASL0
GLOBAL DECODER
1455
PRE-DECODER
1451
AXA

FIG.59

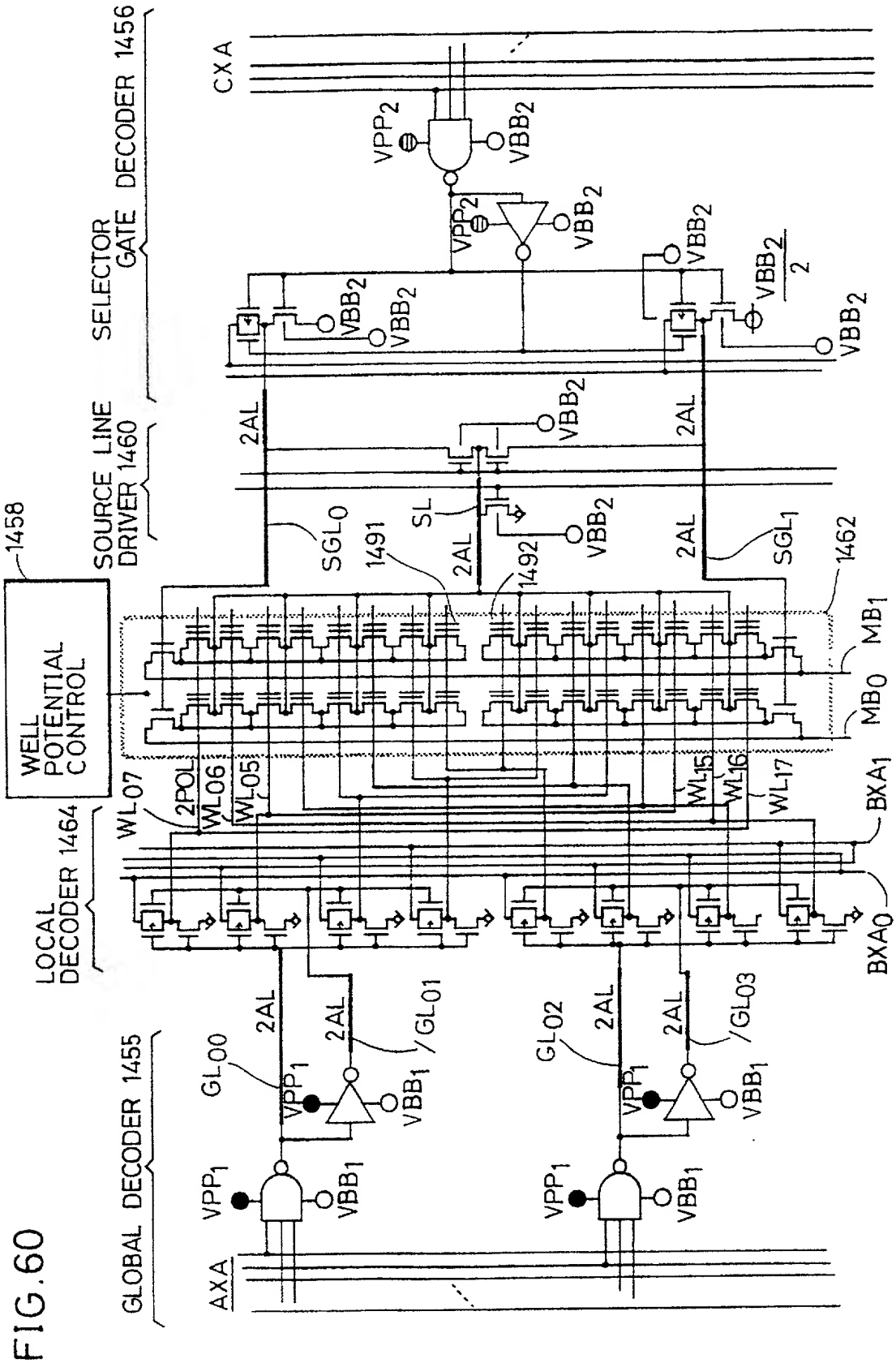

GLOBAL DECODER 1455
LOCAL DECODER 1464
SOURCE LINE DRIVER 1460
SELECTOR GATE DECODER 1456
WELL POTENTIAL CONTROL
1458
CXA
AXA
BXA0
BXA1
MB0
MB1
SGL0
SGL1
SL
1491
1492
1462
2AL
2POL
WL05
WL06
WL07
WL15
WL16
WL17
GL00
GL01
GL02
GL03
VPP1
VPP2
VBB1
VBB2
VBB2/2

FIG.60

FIG. 61

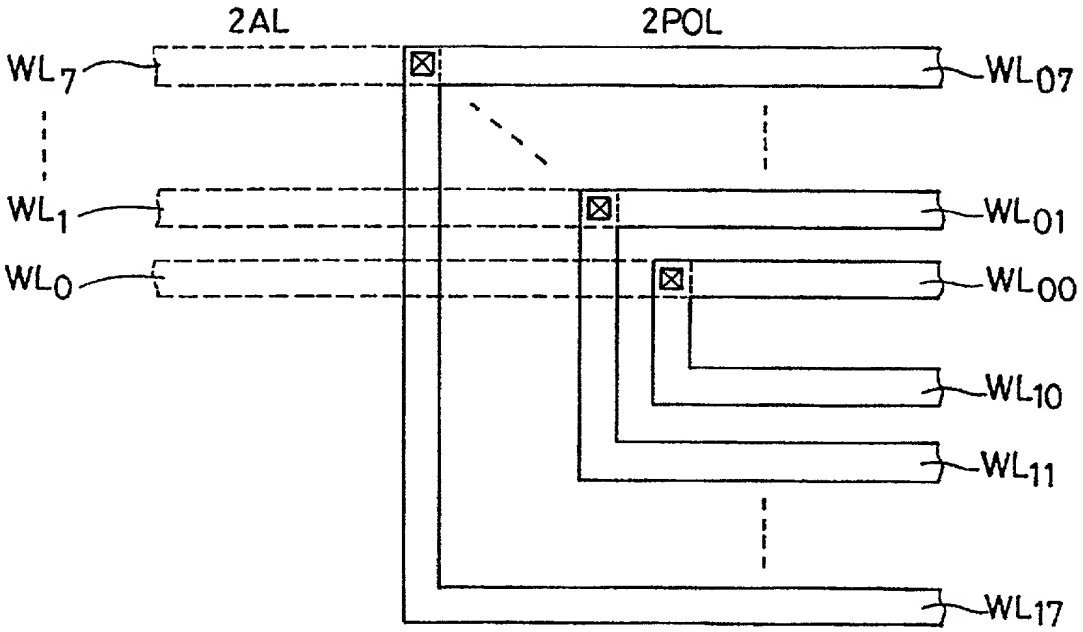
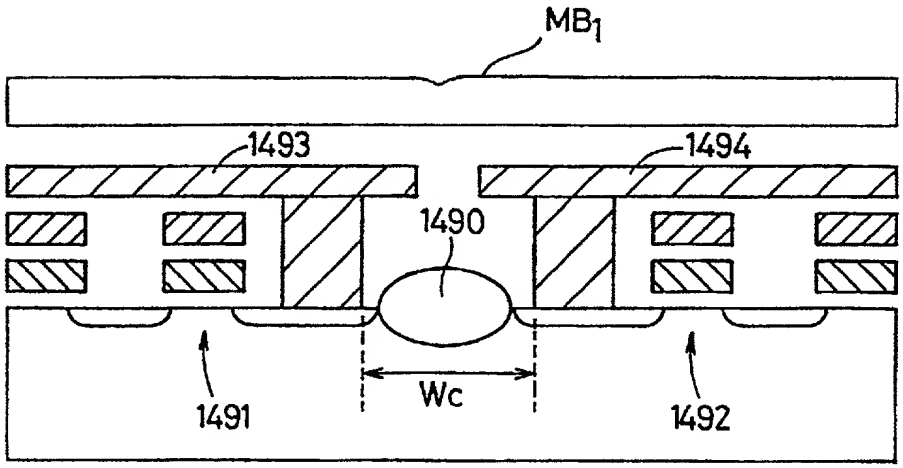

2AL
2POL
WL7
WL1
WL0
WL07
WL01
WL00
WL10
WL11
WL17

FIG. 62


MB1
1493
1494
1490
1491
Wc
1492

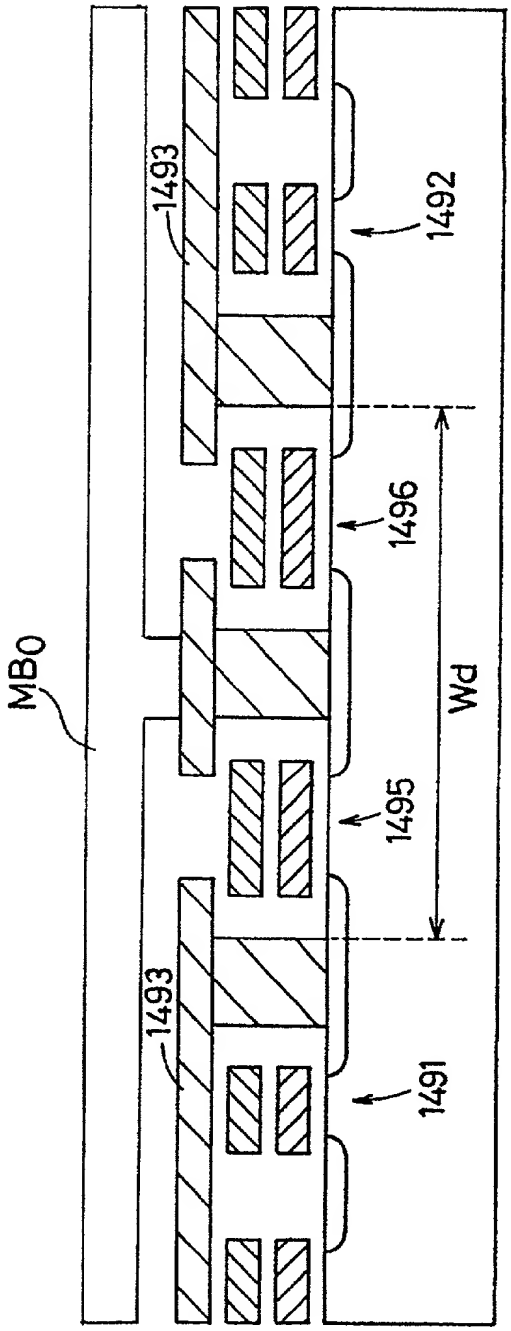


FIG. 63

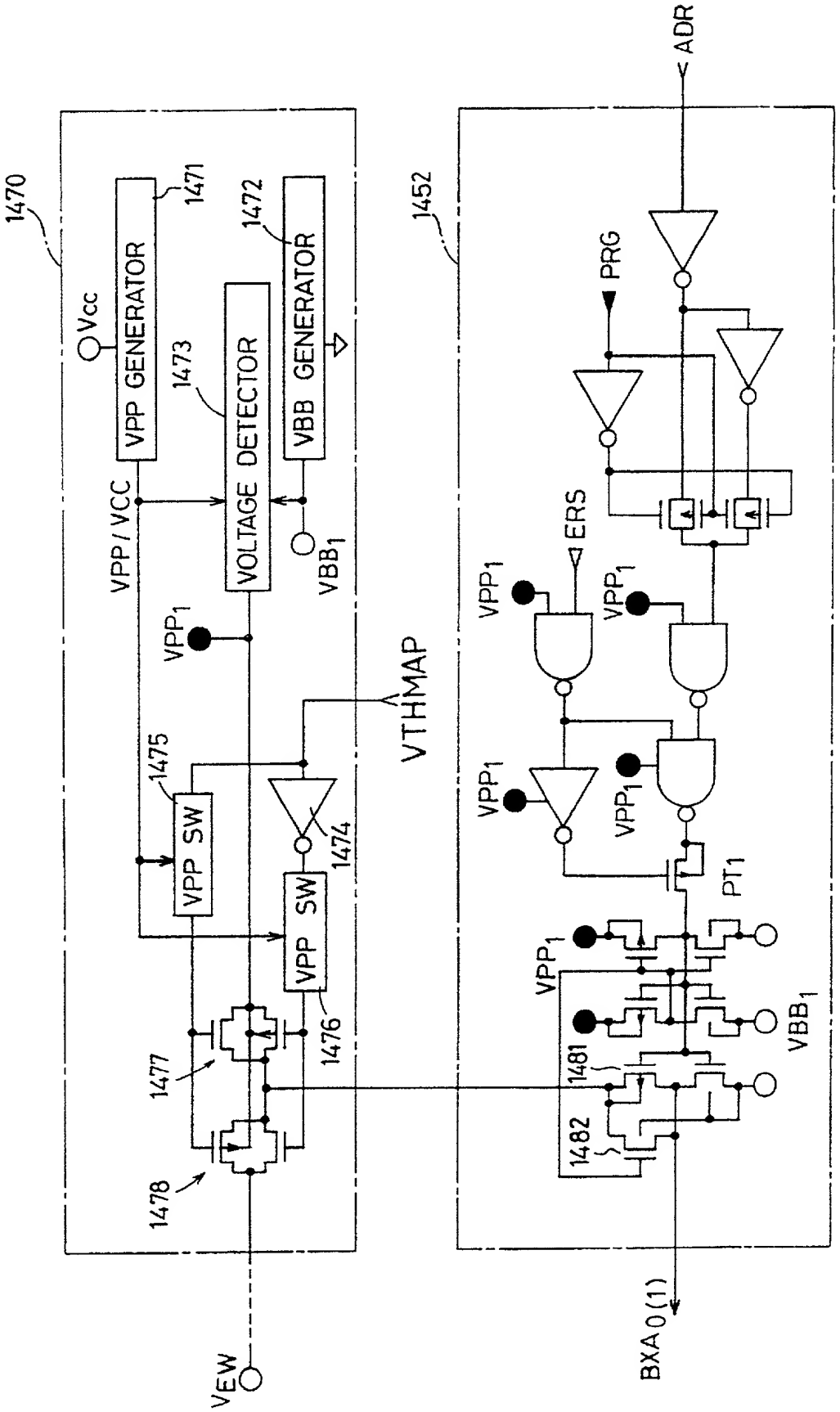
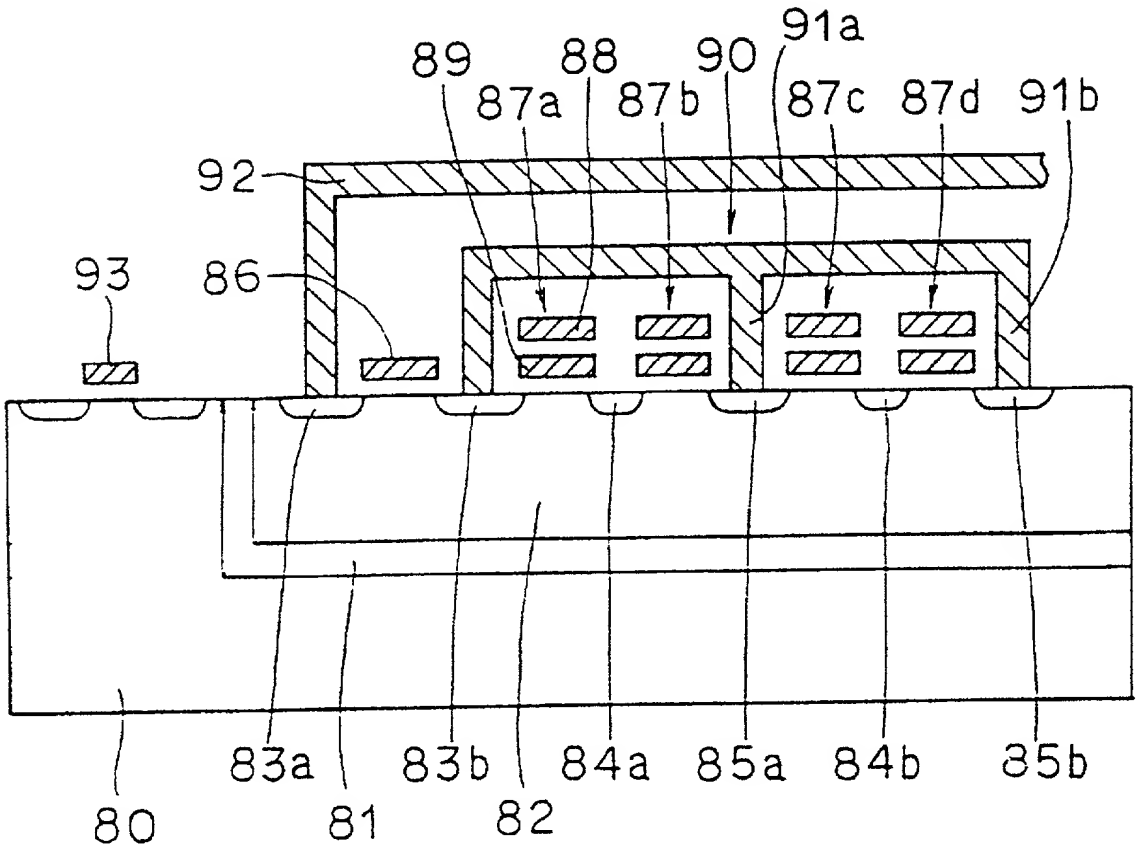
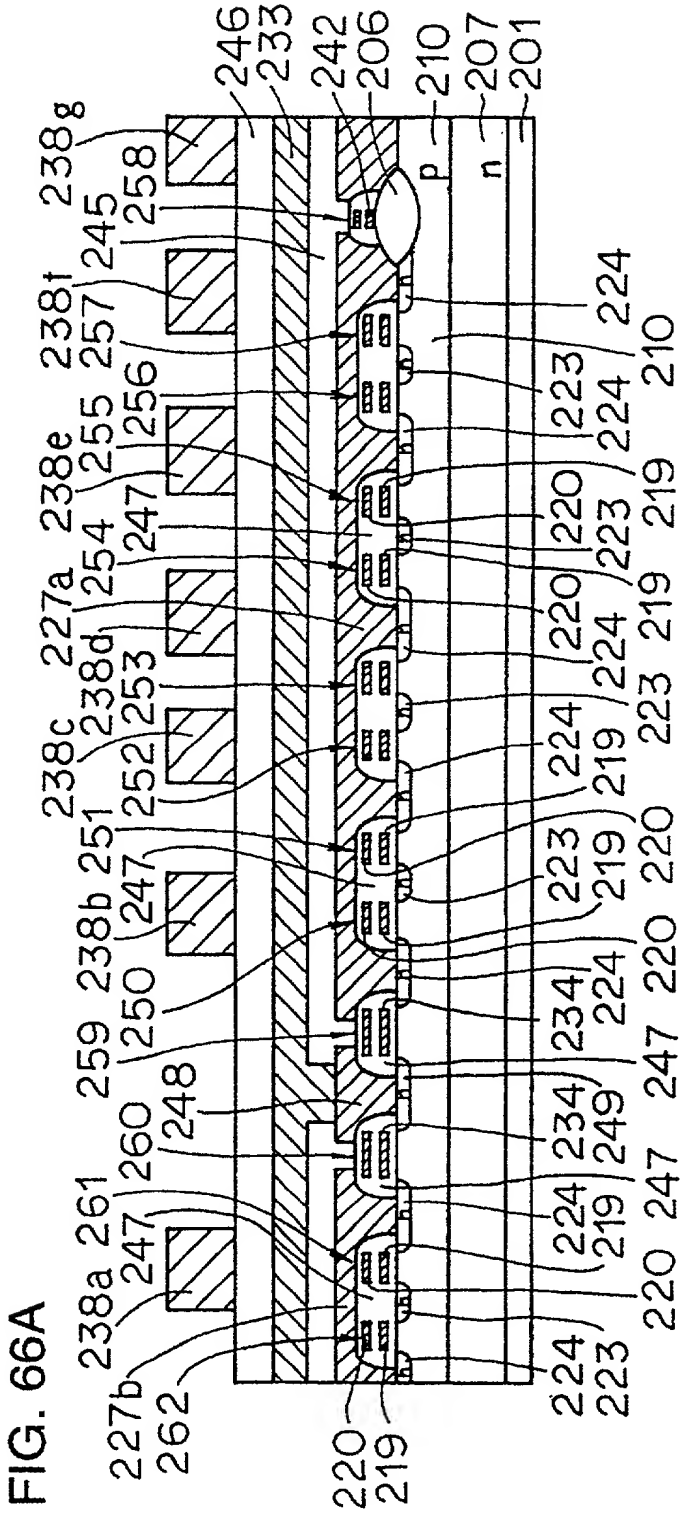

1470
1471
1472
1473
1474
1475
1476
1477
1478
1452
1481
1482
Vcc
VPP GENERATOR
VOLTAGE DETECTOR
VBB GENERATOR
VPP / VCC
VBB1
VPP1
VTHMAP
VPP SW
VPP SW
VEW
ADR
PRG
ERS
PT1
BXA0(1)

FIG. 64

FIG. 65


89
88
90
91a
87a
87b
87c
87d
91b
92
93
86
83a
83b
84a
85a
84b
85b
80
81
82


246
233
242
206
210
207
201
238g
258
245
238f
257
256
238e
255
247
254
227a
238d
253
252
238c
251
247
238b
259
250
248
260
238a
261
247
227b
262
220
219
p
n
224
223
219
220
234
249
FIG. 66A

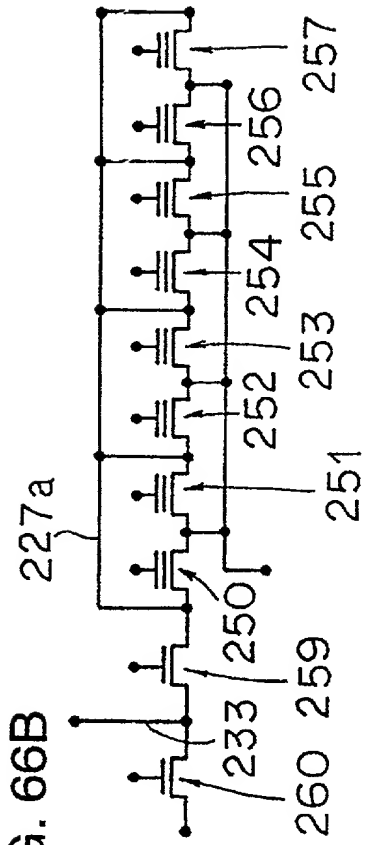

227a
257
256
255
254
253
252
251
250
233
259
260
FIG. 66B

FIG. 67

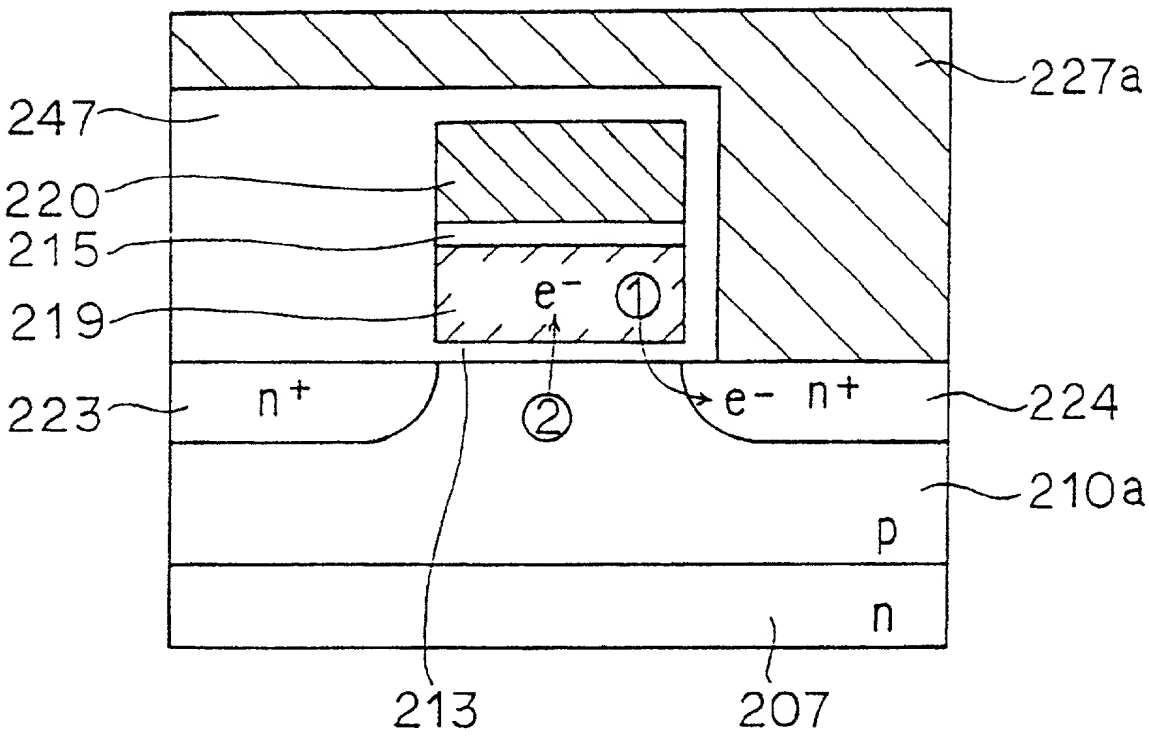


FIG. 68

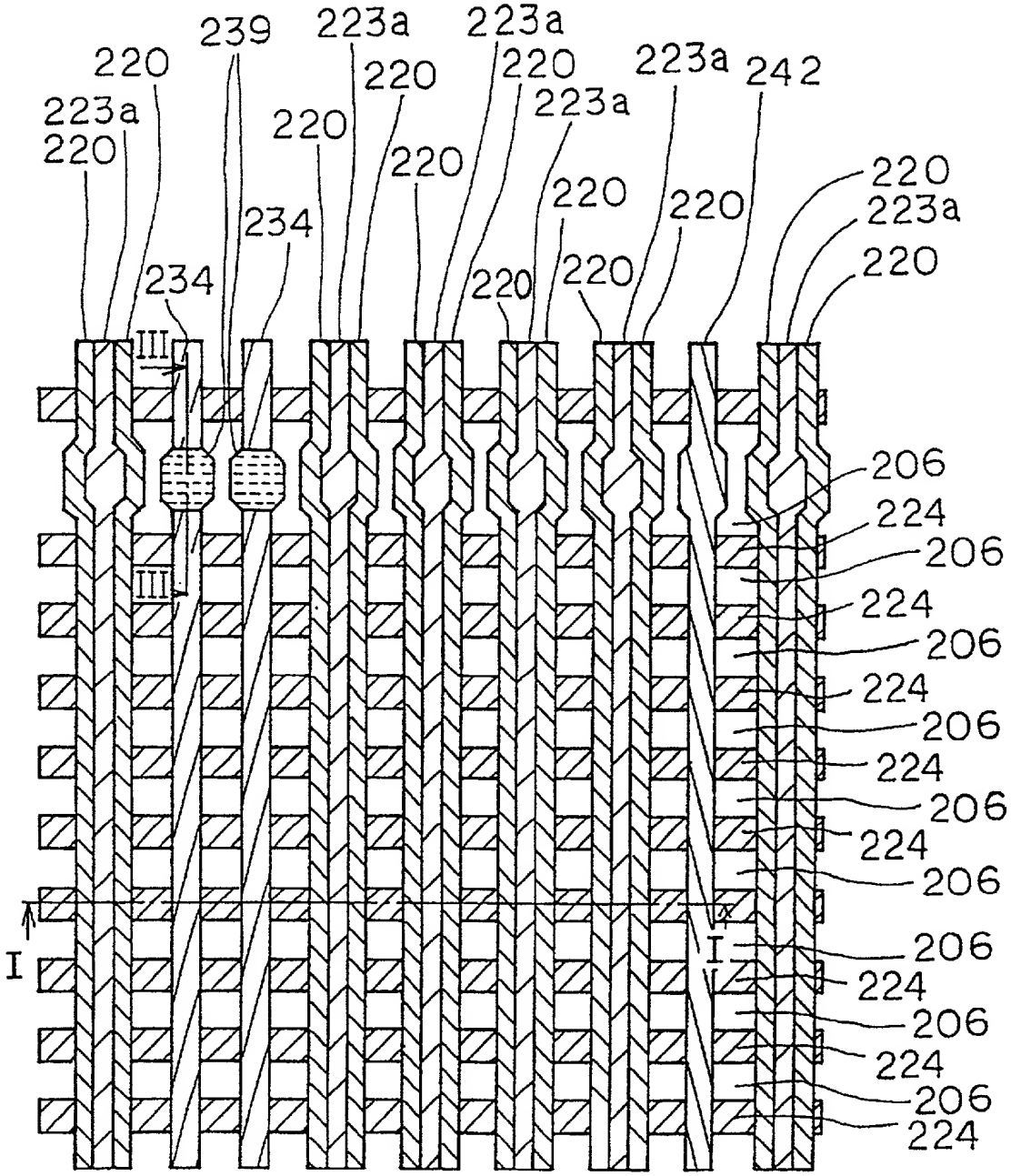


FIG. 69

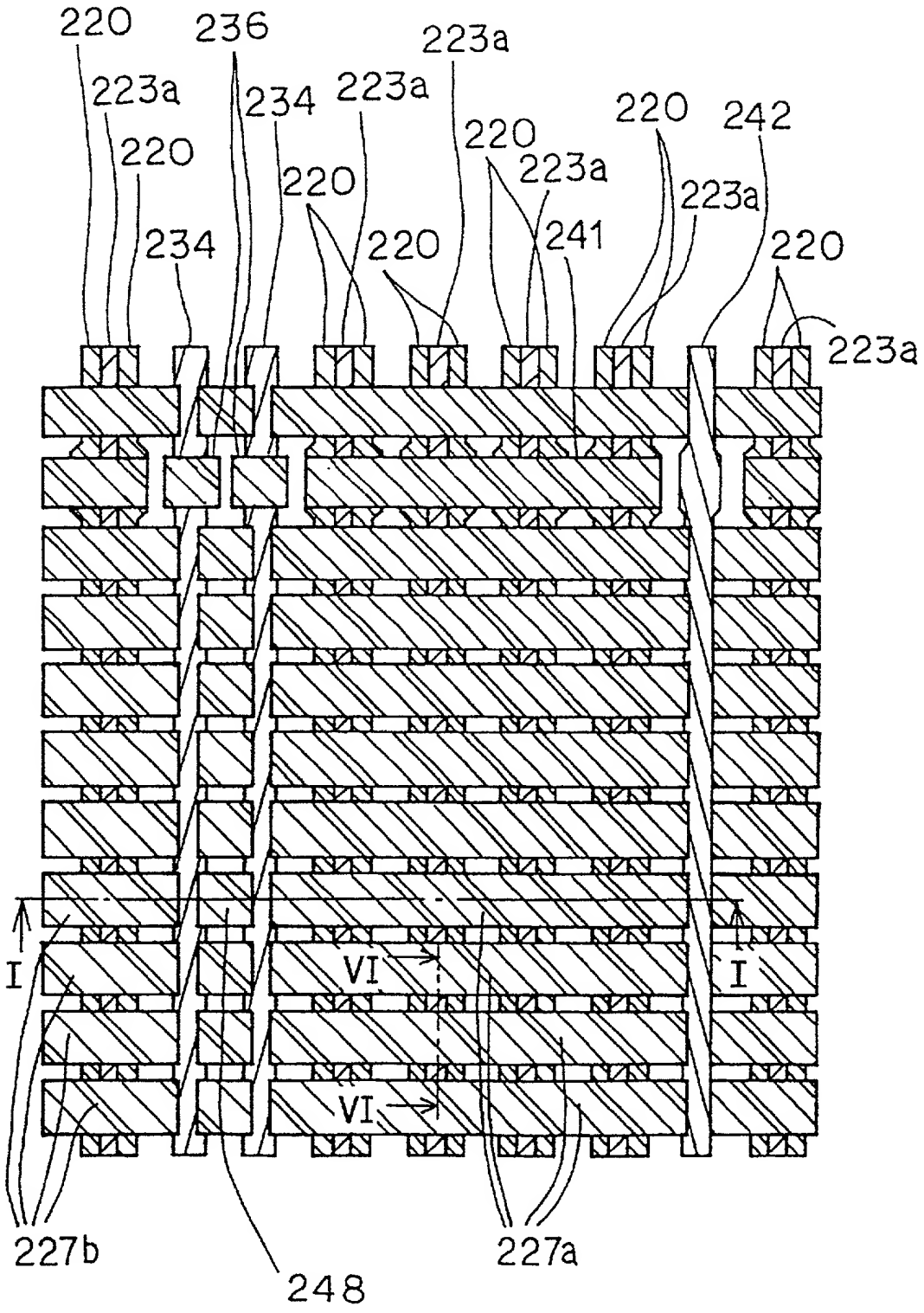

220
236
223a
223a
234
223a
220
220
220
242
220
223a
223a
234
220
241
220
223a
I
VI
I
VI
227b
248
227a

FIG. 70

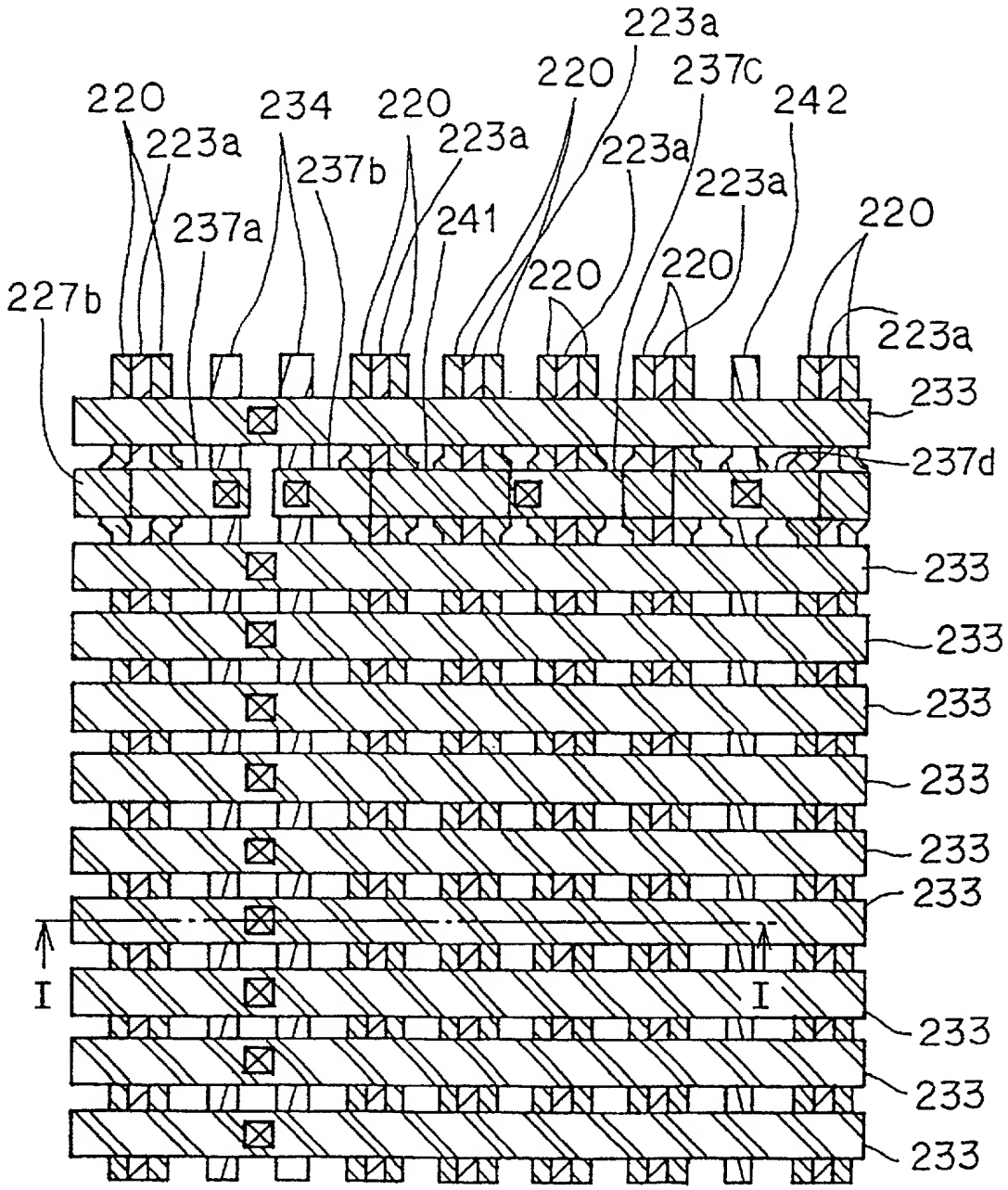
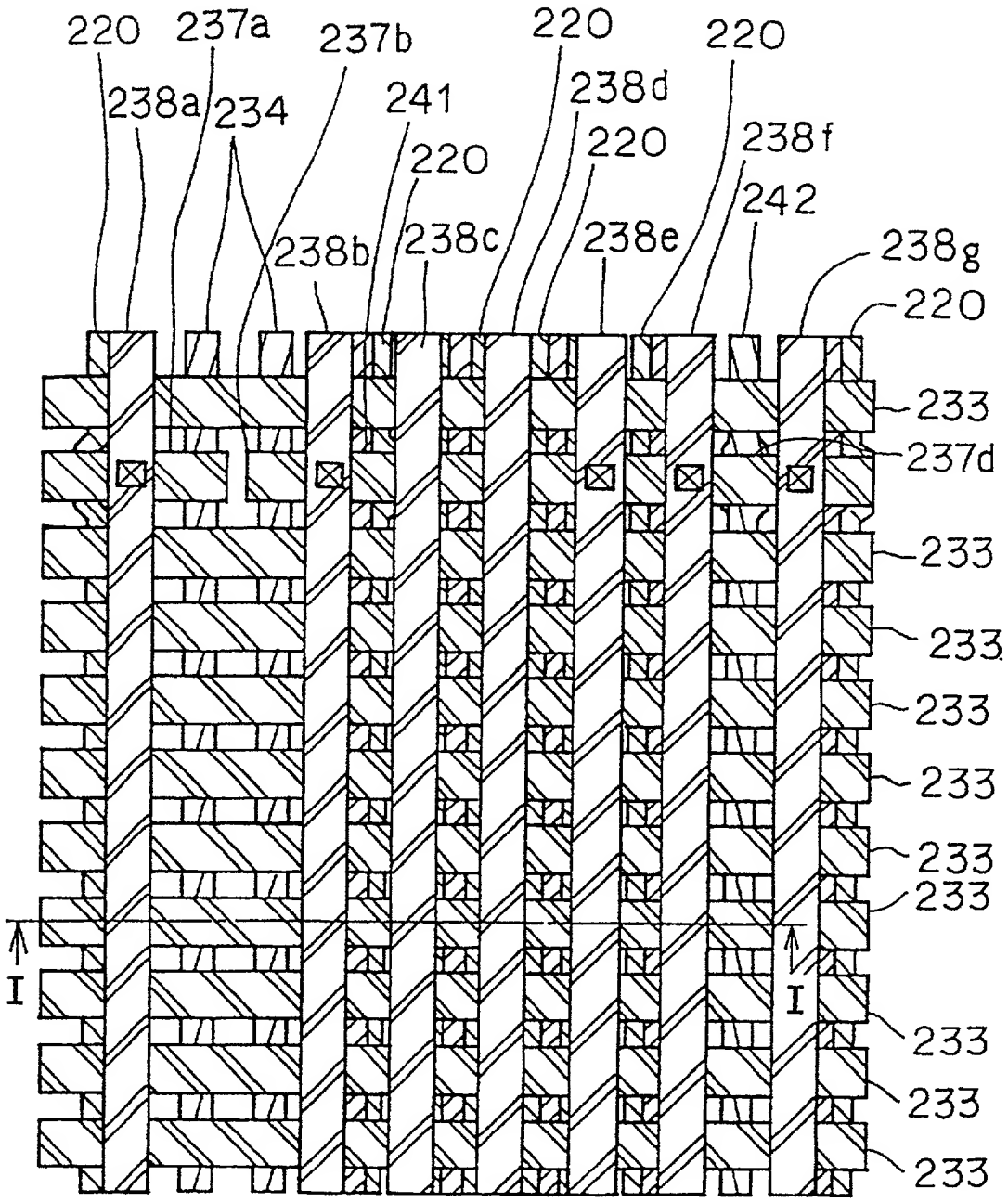

223a
220
237c
242
220
234
220
223a
223a
223a
223a
237b
237a
241
220
220
220
227b
223a
233
237d
233
233
233
233
233
233
I
I
233
233
233

FIG. 71


220
237a
237b
220
220
238a
234
241
238d
220
238f
220
242
238b
238c
238e
238g
220
233
237d
233
233
233
233
233
233
I
I
233
233
233

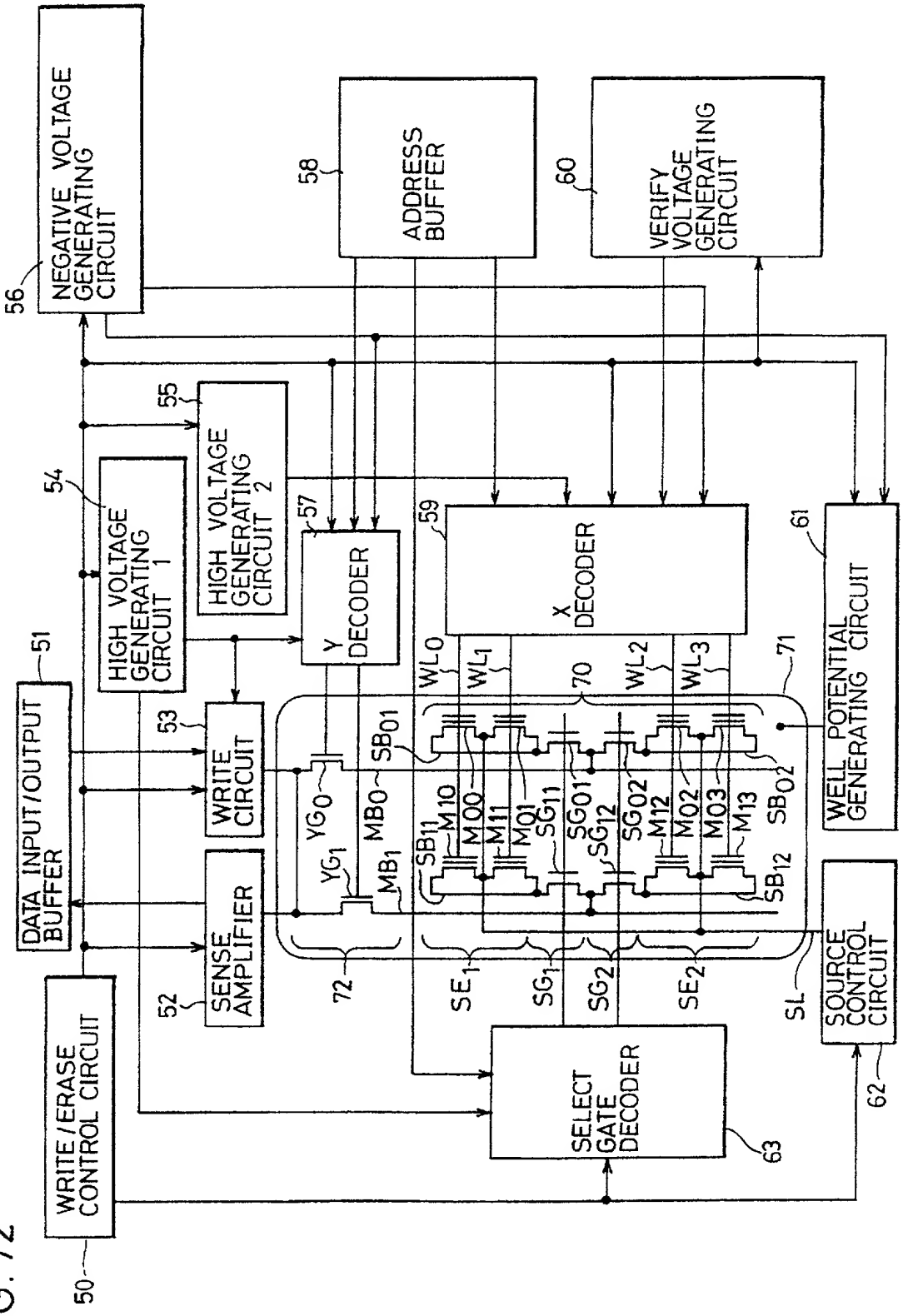

NEGATIVE VOLTAGE GENERATING CIRCUIT
56
ADDRESS BUFFER
58
VERIFY VOLTAGE GENERATING CIRCUIT
60
HIGH VOLTAGE GENERATING CIRCUIT 2
55
HIGH VOLTAGE GENERATING CIRCUIT 1
54
Y DECODER
57
X DECODER
59
WELL POTENTIAL GENERATING CIRCUIT
61
DATA INPUT/OUTPUT BUFFER
51
WRITE CIRCUIT
53
SENSE AMPLIFIER
52
WRITE/ERASE CONTROL CIRCUIT
50
SOURCE CONTROL CIRCUIT
62
SELECT GATE DECODER
63
WL0
WL1
WL2
WL3
70
71
72
YG0
YG1
MB0
MB1
SB01
SB02
SB11
SB12
M00
M01
M02
M03
M10
M11
M12
M13
SG01
SG02
SG11
SG12
SE1
SE2
SG1
SG2
SL

FIG. 72

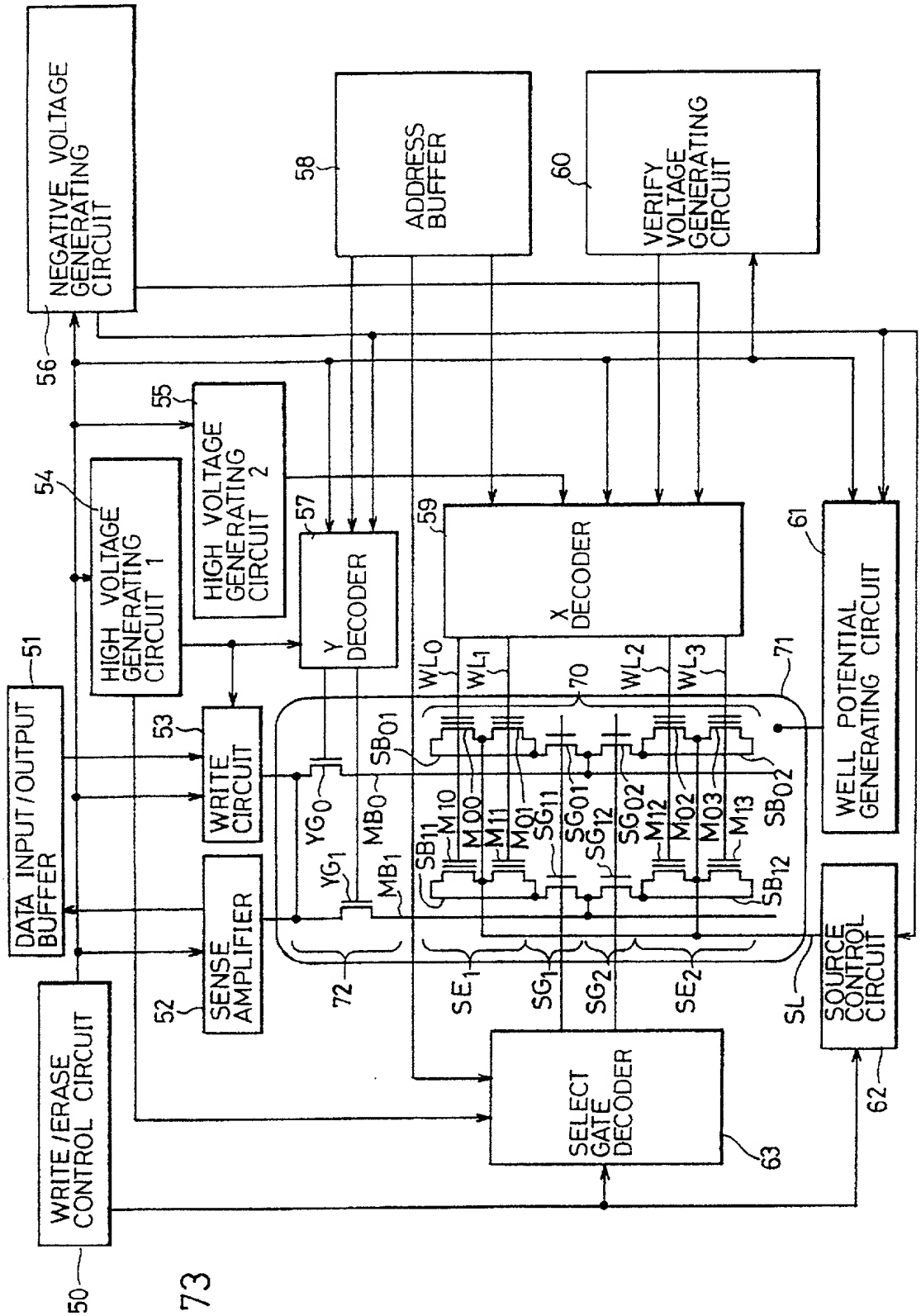

NEGATIVE VOLTAGE GENERATING CIRCUIT
ADDRESS BUFFER
VERIFY VOLTAGE GENERATING CIRCUIT
HIGH VOLTAGE GENERATING CIRCUIT 1
HIGH VOLTAGE GENERATING CIRCUIT 2
Y DECODER
X DECODER
WELL POTENTIAL GENERATING CIRCUIT
DATA INPUT/OUTPUT BUFFER
WRITE CIRCUIT
SENSE AMPLIFIER
SOURCE CONTROL CIRCUIT
WRITE/ERASE CONTROL CIRCUIT
SELECT GATE DECODER
WL0
WL1
WL2
WL3
YG0
YG1
MB0
MB1
SB01
SB02
SB11
SB12
M00
M01
M02
M03
M10
M11
M12
M13
SG01
SG02
SG11
SG12
SE1
SE2
SG1
SG2
SL
50
51
52
53
54
55
56
57
58
59
60
61
62
63
70
71
72

FIG. 73

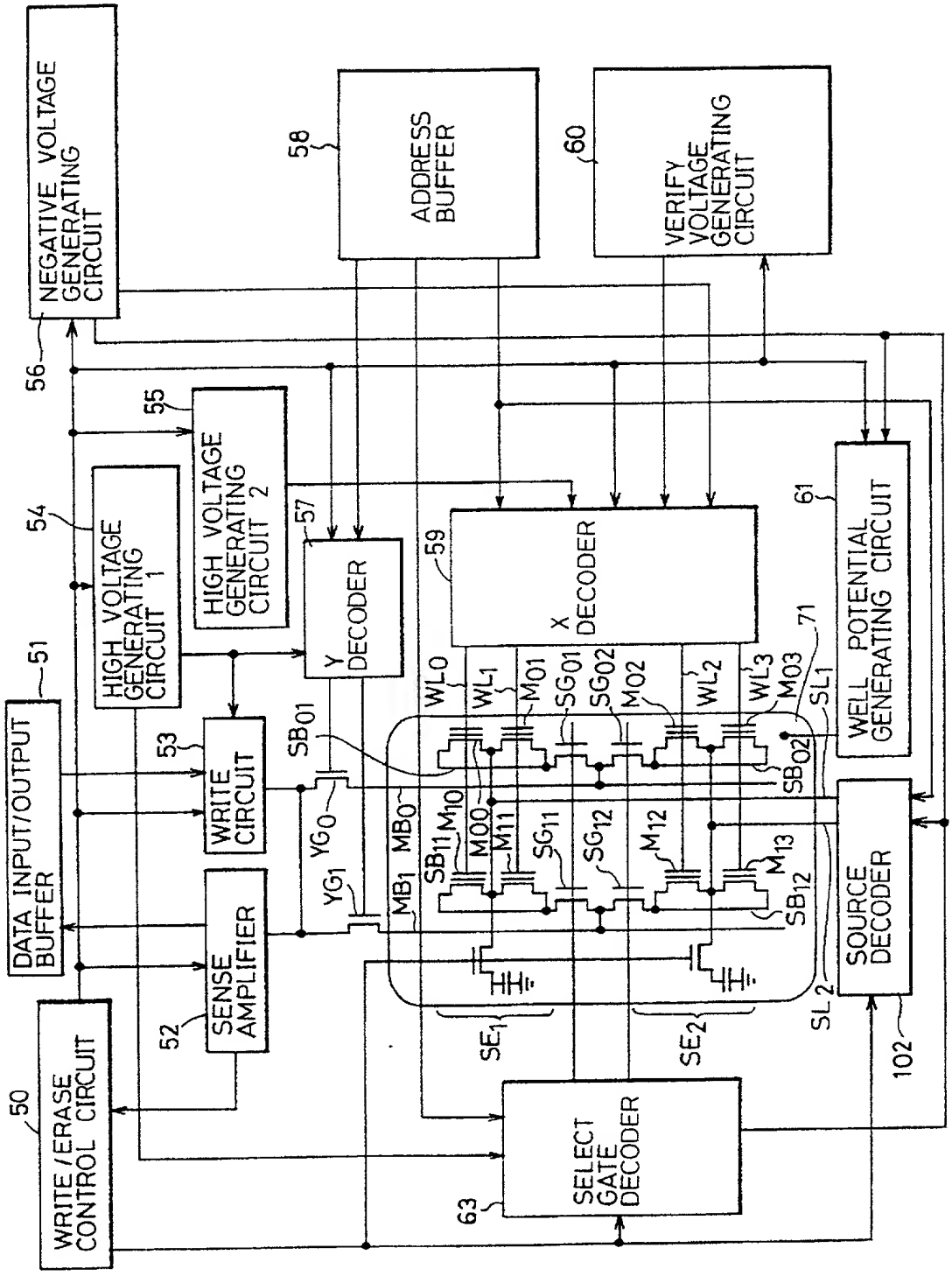

NEGATIVE VOLTAGE GENERATING CIRCUIT
56
ADDRESS BUFFER
58
VERIFY VOLTAGE GENERATING CIRCUIT
60
HIGH VOLTAGE GENERATING CIRCUIT 2
55
HIGH VOLTAGE GENERATING CIRCUIT 1
54
Y DECODER
57
X DECODER
59
WELL POTENTIAL GENERATING CIRCUIT
61
DATA INPUT/OUTPUT BUFFER
51
WRITE CIRCUIT
53
SENSE AMPLIFIER
52
WRITE/ERASE CONTROL CIRCUIT
50
SOURCE DECODER
102
SELECT GATE DECODER
63
WL0
WL1
WL2
WL3
M01
M02
M03
SG01
SG02
SG11
SG12
M00
M10
M11
M12
M13
SB01
SB02
SB11
SB12
YG0
YG1
MB0
MB1
SE1
SE2
SL1
SL2
71

FIG. 74

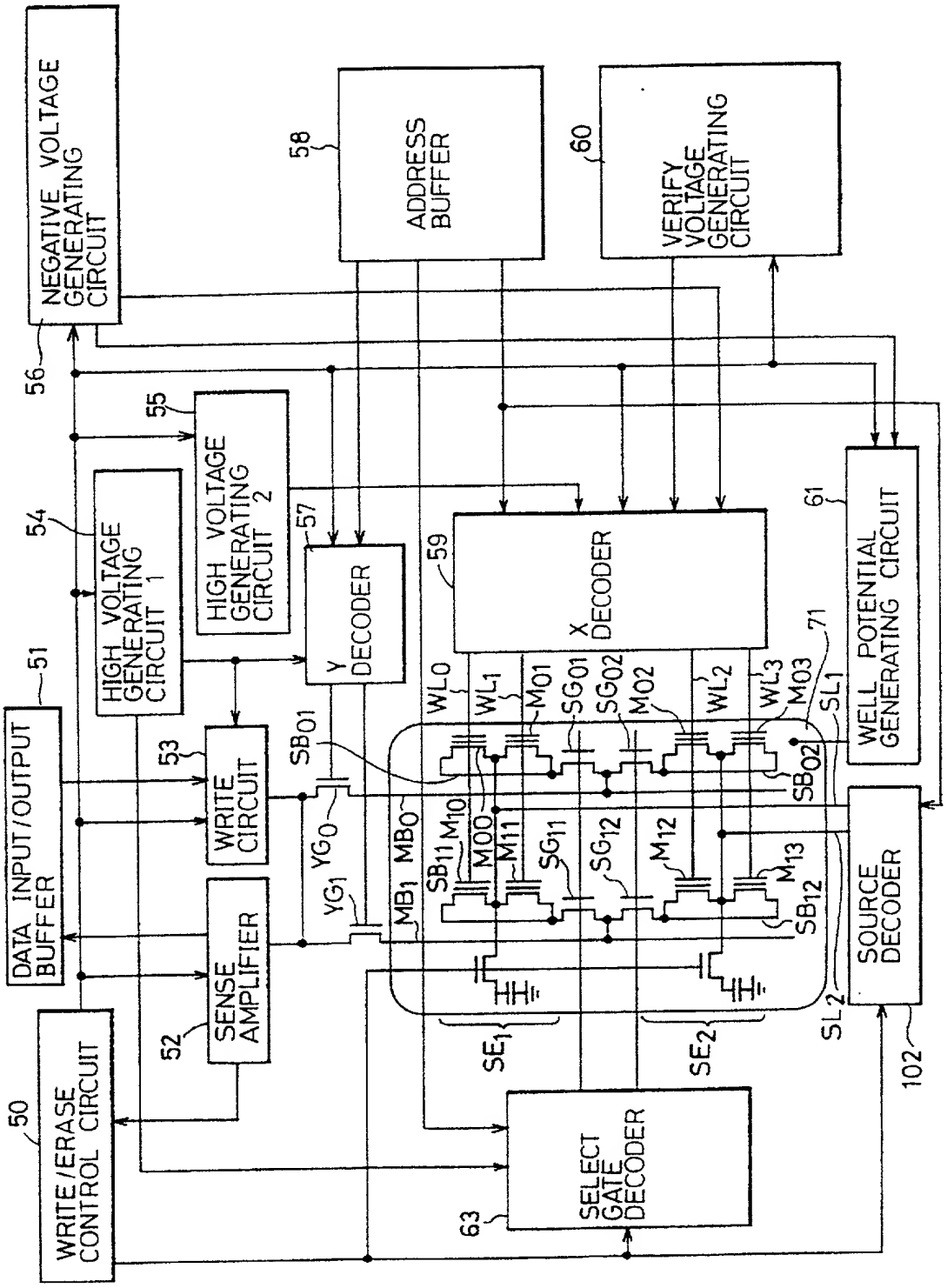

NEGATIVE VOLTAGE GENERATING CIRCUIT
56
ADDRESS BUFFER
58
VERIFY VOLTAGE GENERATING CIRCUIT
60
HIGH VOLTAGE GENERATING CIRCUIT 1
54
HIGH VOLTAGE GENERATING CIRCUIT 2
55
Y DECODER
57
X DECODER
59
WELL POTENTIAL GENERATING CIRCUIT
61
DATA INPUT/OUTPUT BUFFER
51
WRITE CIRCUIT
53
SENSE AMPLIFIER
52
WRITE/ERASE CONTROL CIRCUIT
50
SELECT GATE DECODER
63
SOURCE DECODER
102
WL0
WL1
WL2
WL3
M01
M02
M03
SG01
SG02
SG11
SG12
M00
M10
M11
M12
M13
SB01
SB02
SB11
SB12
SL1
SL2
YG0
YG1
MB0
MB1
SE1
SE2
71

FIG. 75

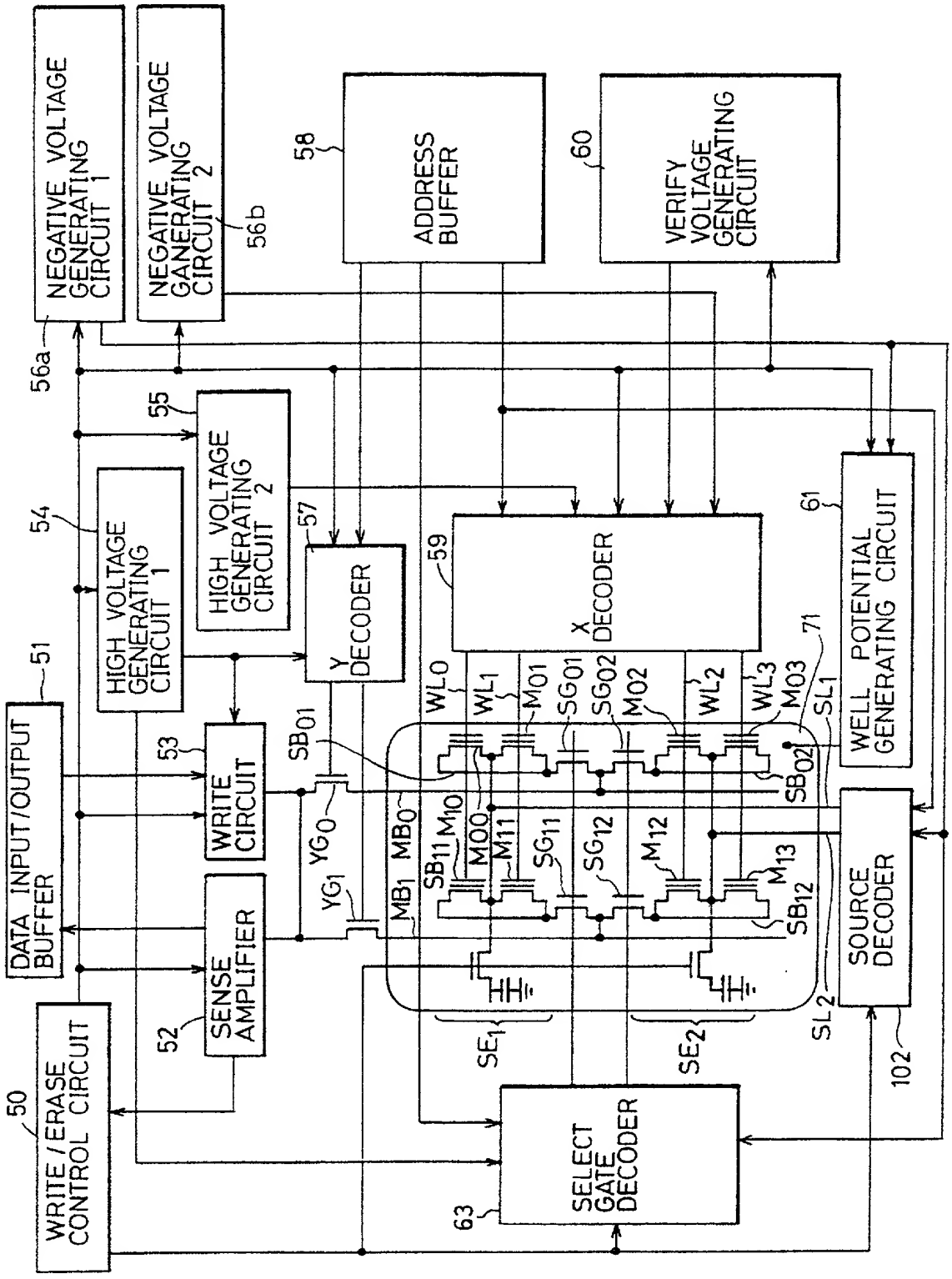

NEGATIVE VOLTAGE GENERATING CIRCUIT 1
NEGATIVE VOLTAGE GANERATING CIRCUIT 2
56a
56b
ADDRESS BUFFER
58
VERIFY VOLTAGE GENERATING CIRCUIT
60
HIGH VOLTAGE GENERATING CIRCUIT 1
54
HIGH VOLTAGE GENERATING CIRCUIT 2
55
Y DECODER
57
X DECODER
59
WELL POTENTIAL GENERATING CIRCUIT
61
DATA INPUT/OUTPUT BUFFER
51
WRITE CIRCUIT
53
SENSE AMPLIFIER
52
WRITE/ERASE CONTROL CIRCUIT
50
SELECT GATE DECODER
63
SOURCE DECODER
102
WL0
WL1
WL2
WL3
M01
M02
M03
SG01
SG02
SB01
SB02
SL1
SL2
YG0
YG1
MB0
MB1
SB11
M10
M00
M11
SG11
SG12
M12
M13
SB12
SE1
SE2
71

FIG. 76

FIG. 77

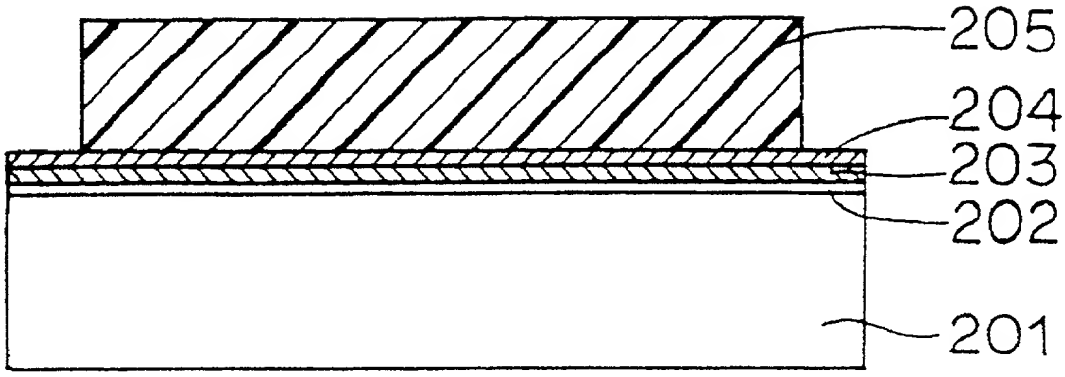


FIG. 78

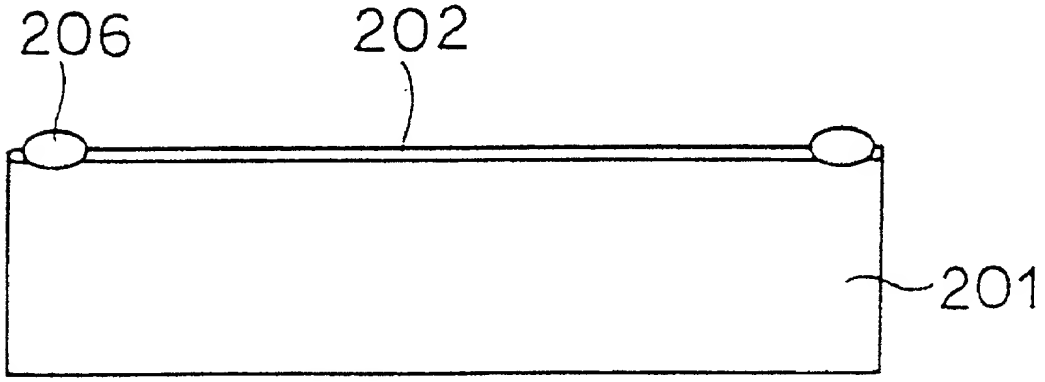


FIG. 79

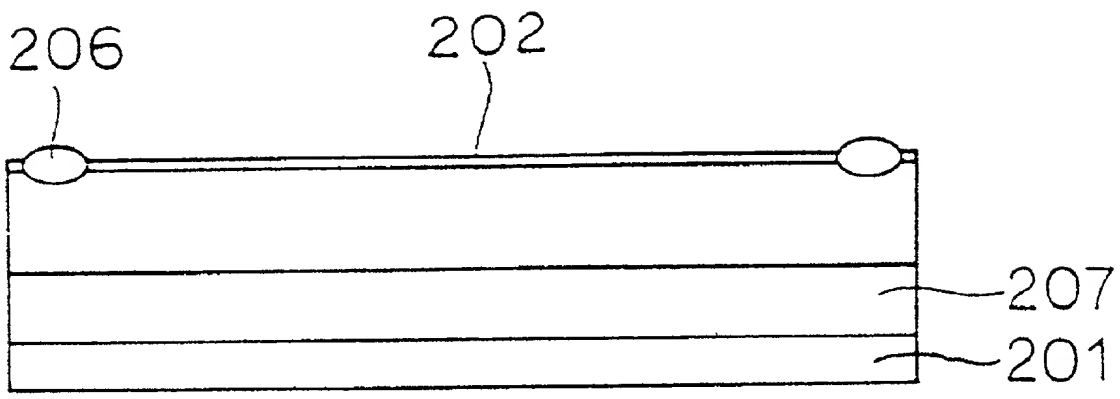


FIG. 80

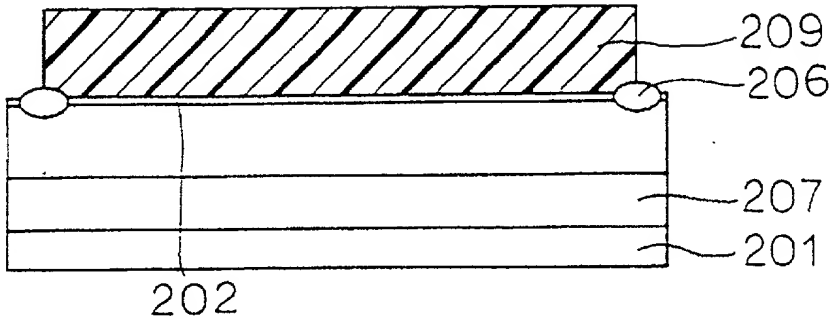


FIG. 81

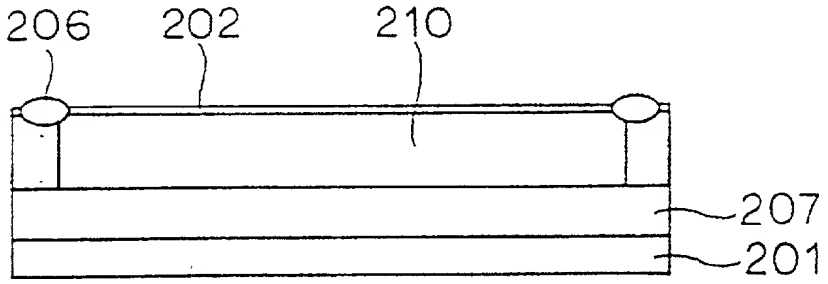


FIG. 82

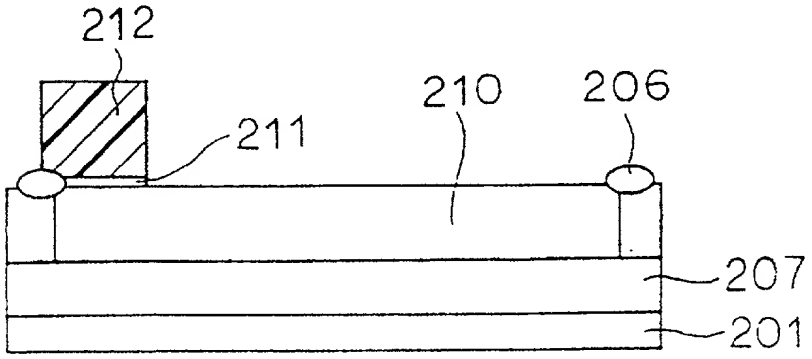


FIG. 83

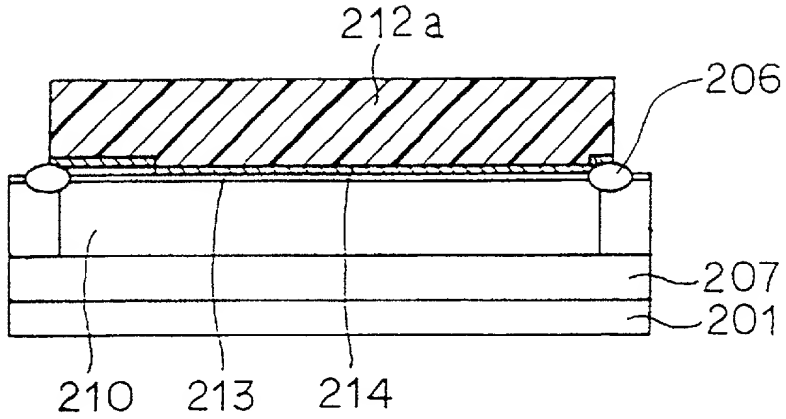


FIG. 84

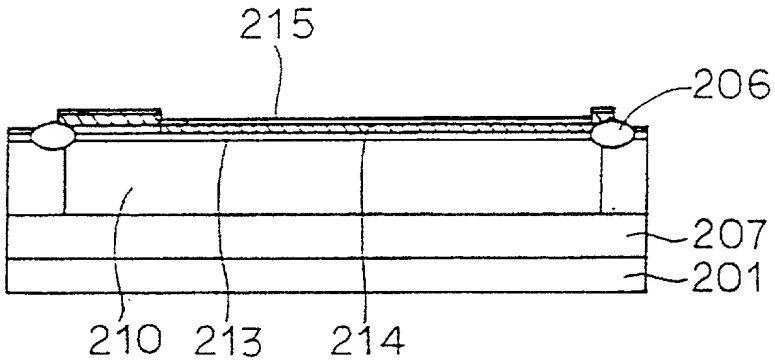


FIG. 85

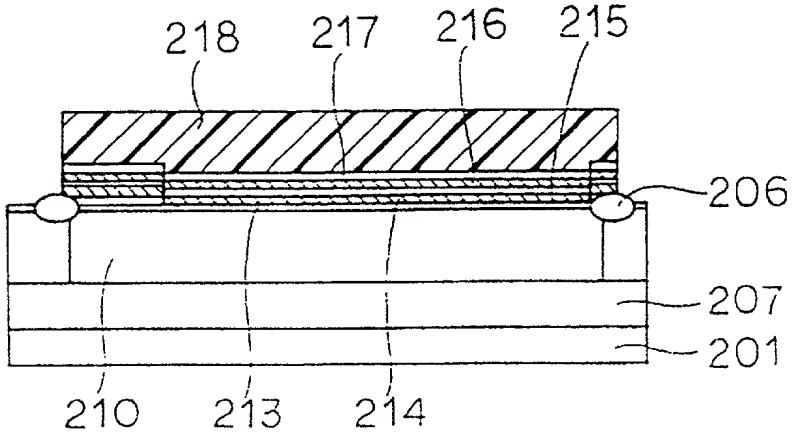


FIG. 86

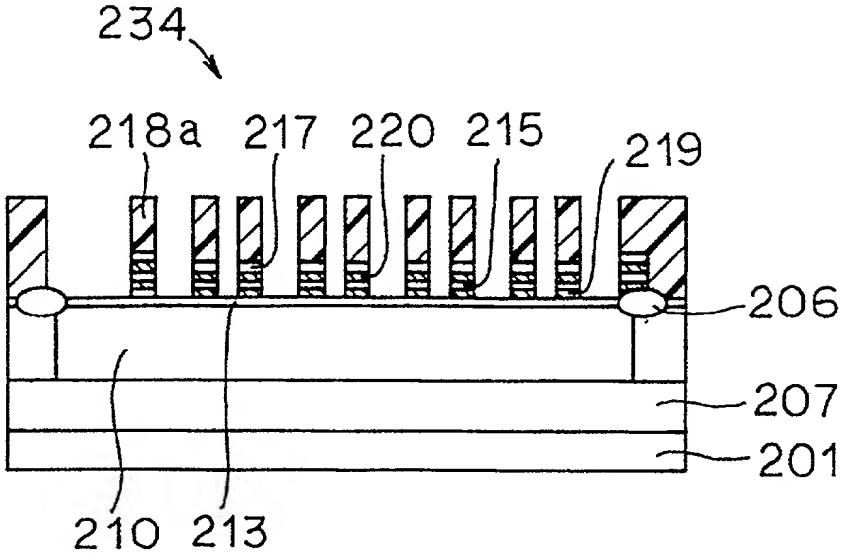


FIG. 87A

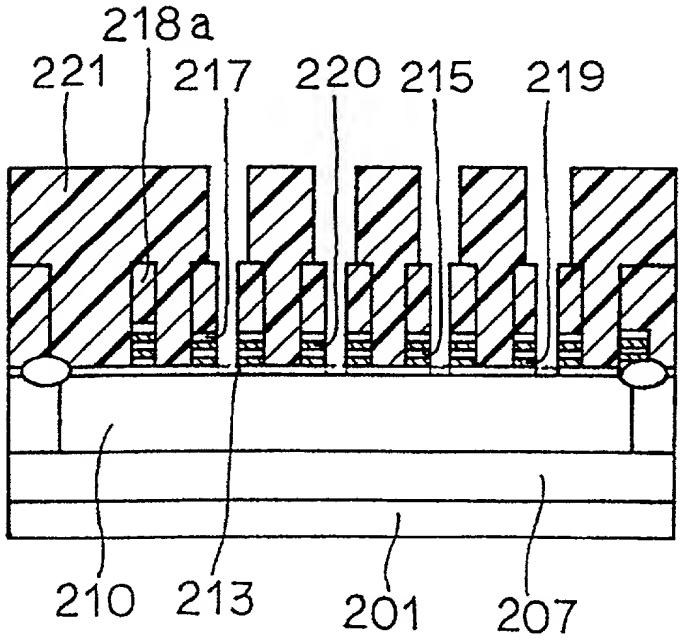


FIG. 87B

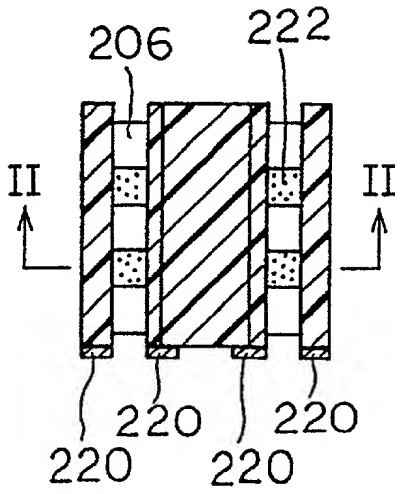


FIG. 88

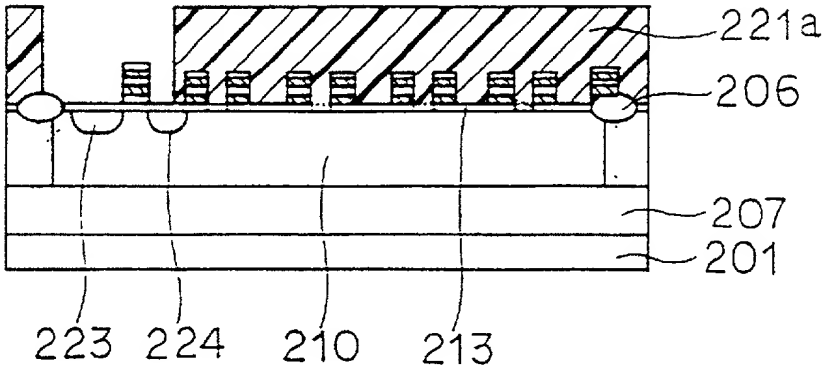


FIG. 89

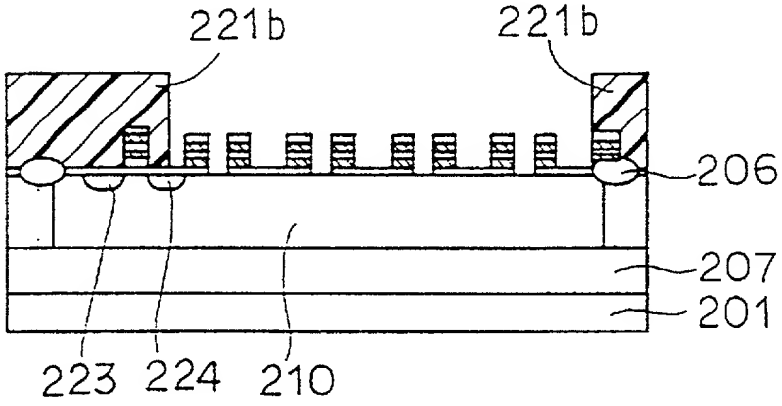


FIG. 90

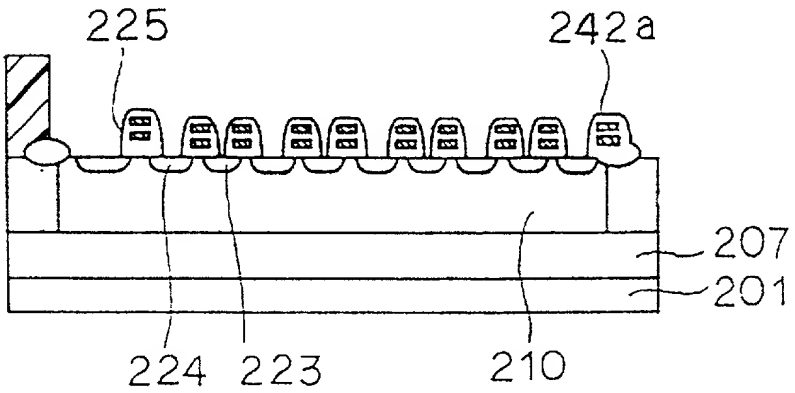


FIG. 91

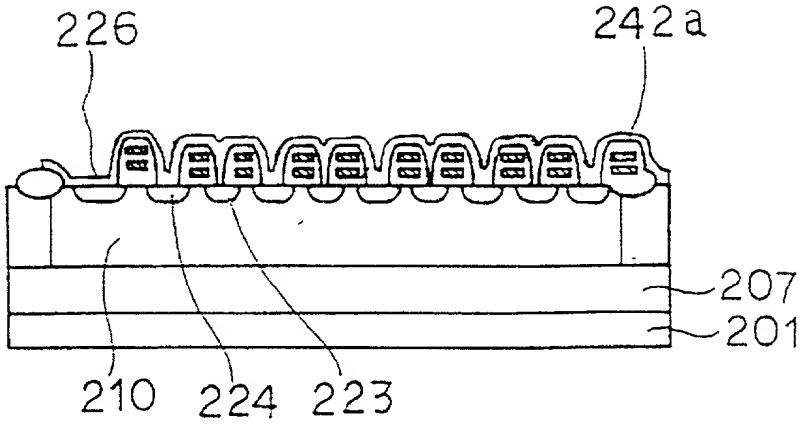


FIG. 92

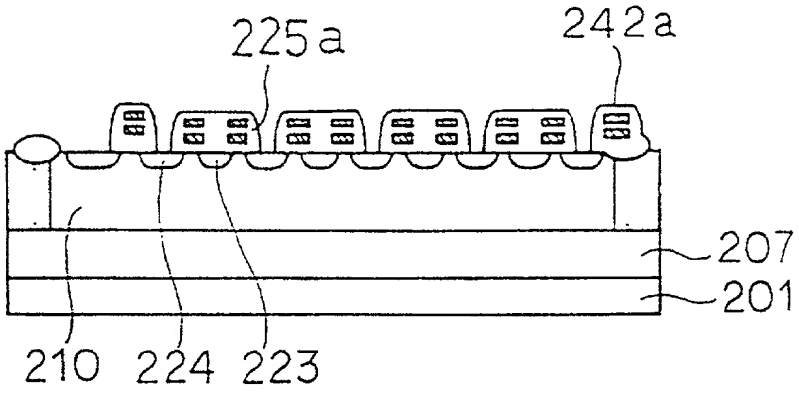


FIG. 93

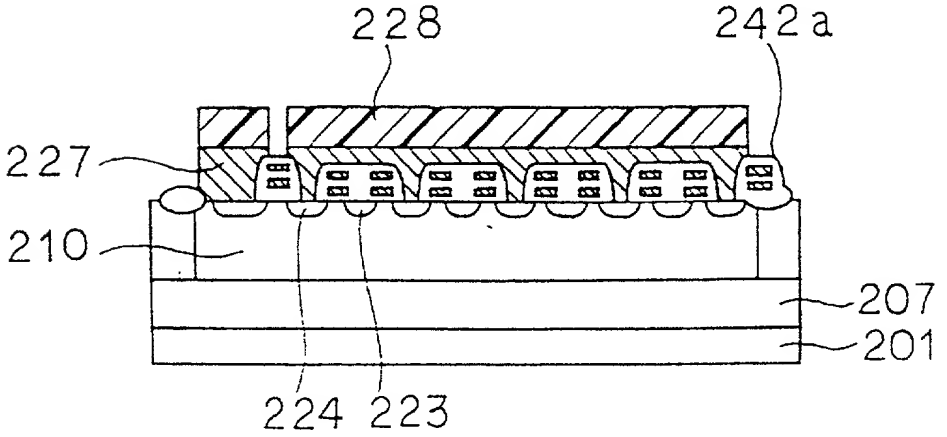


FIG. 94

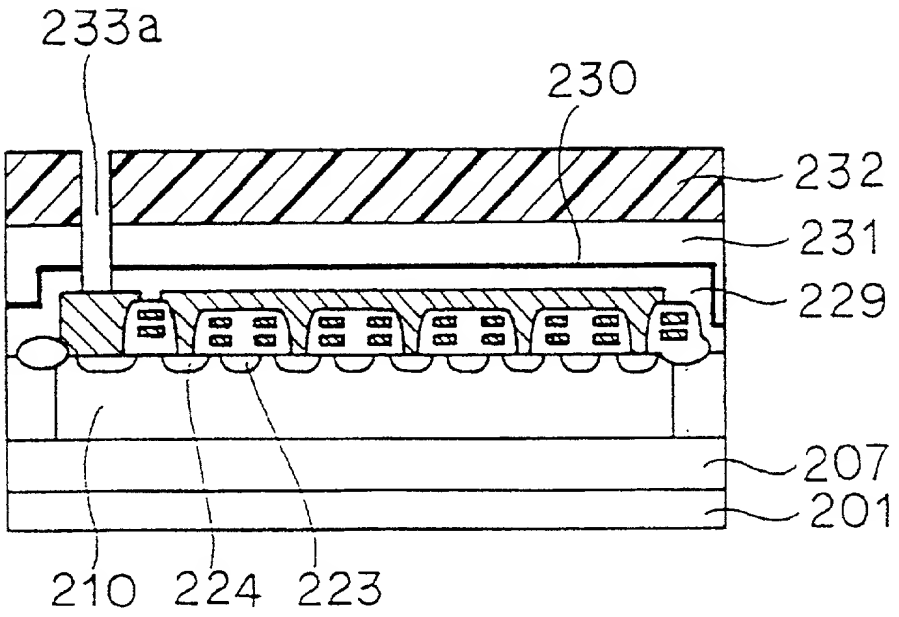

233a
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FIG. 95

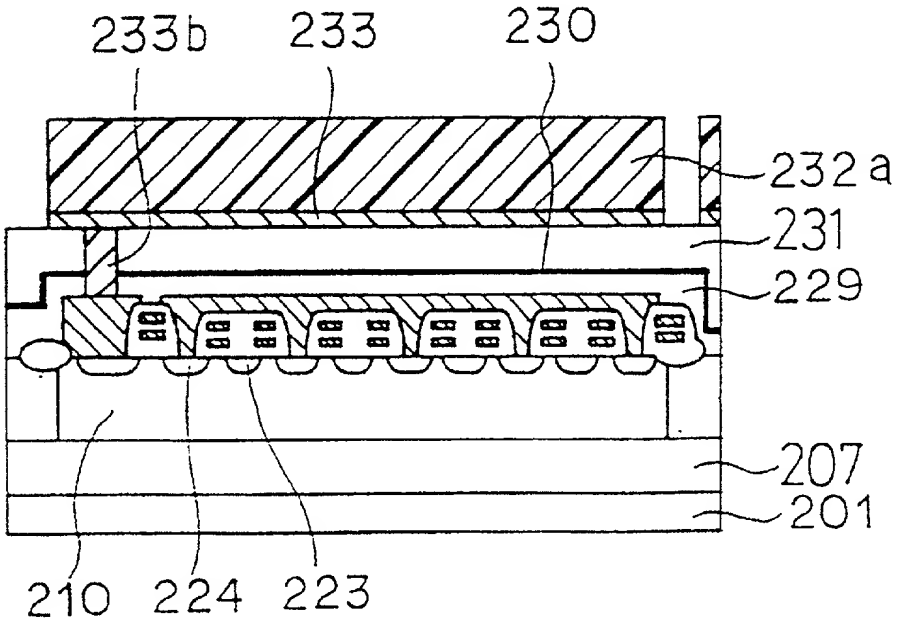
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FIG. 96

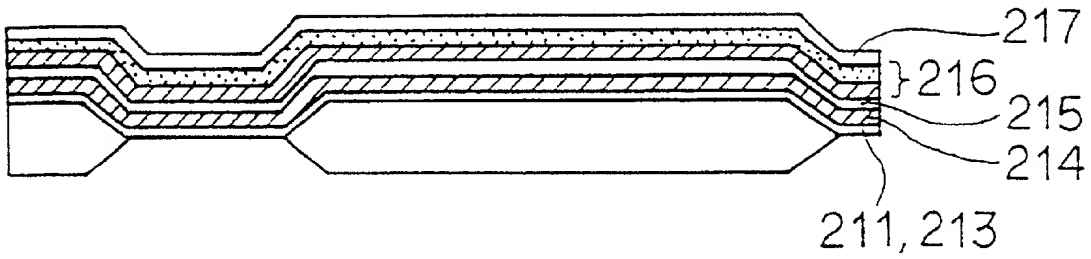


FIG. 97

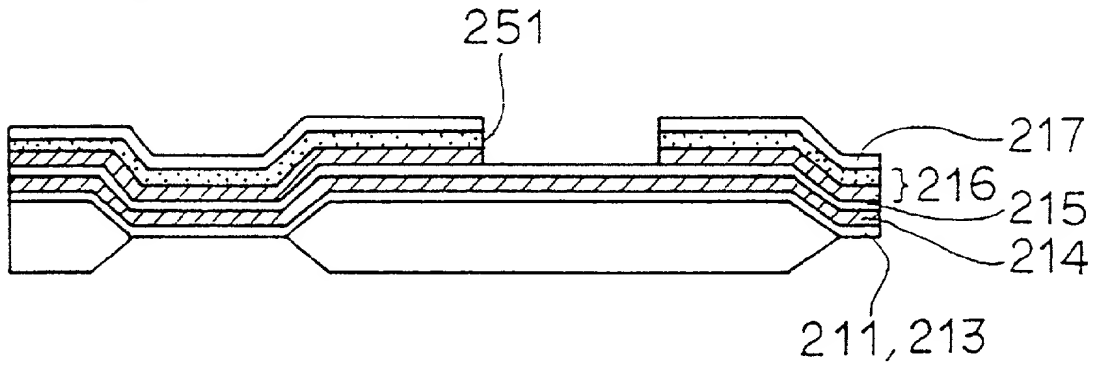


FIG. 98

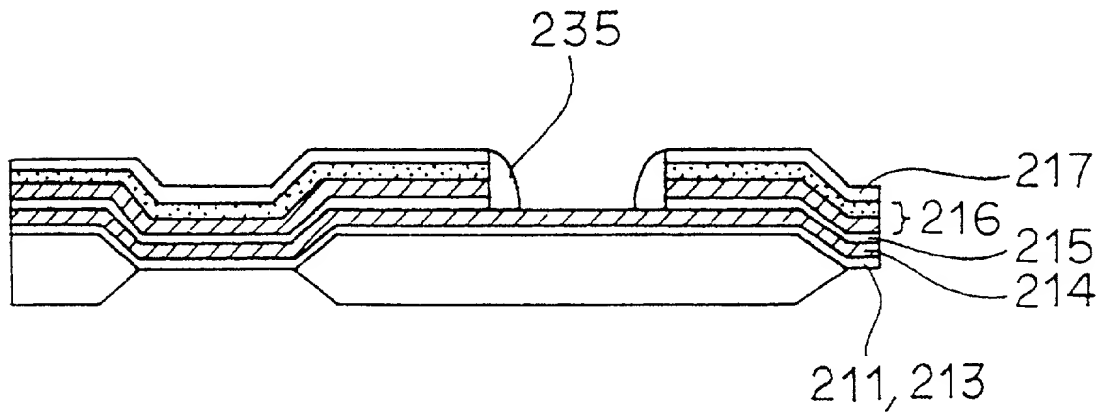


FIG. 99

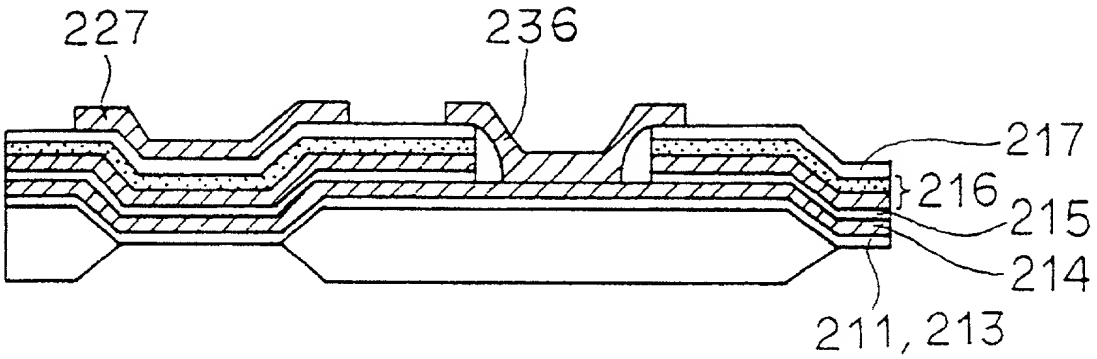


FIG. 100

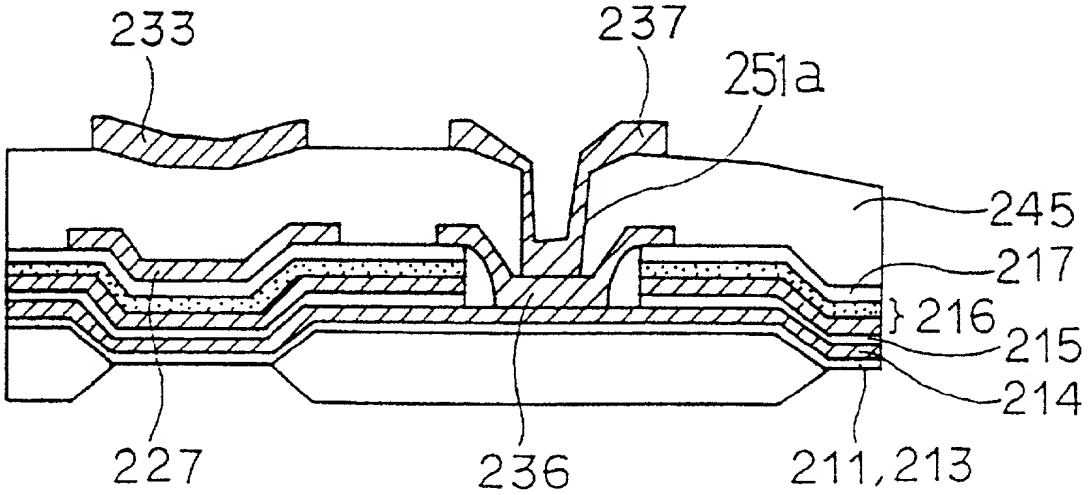
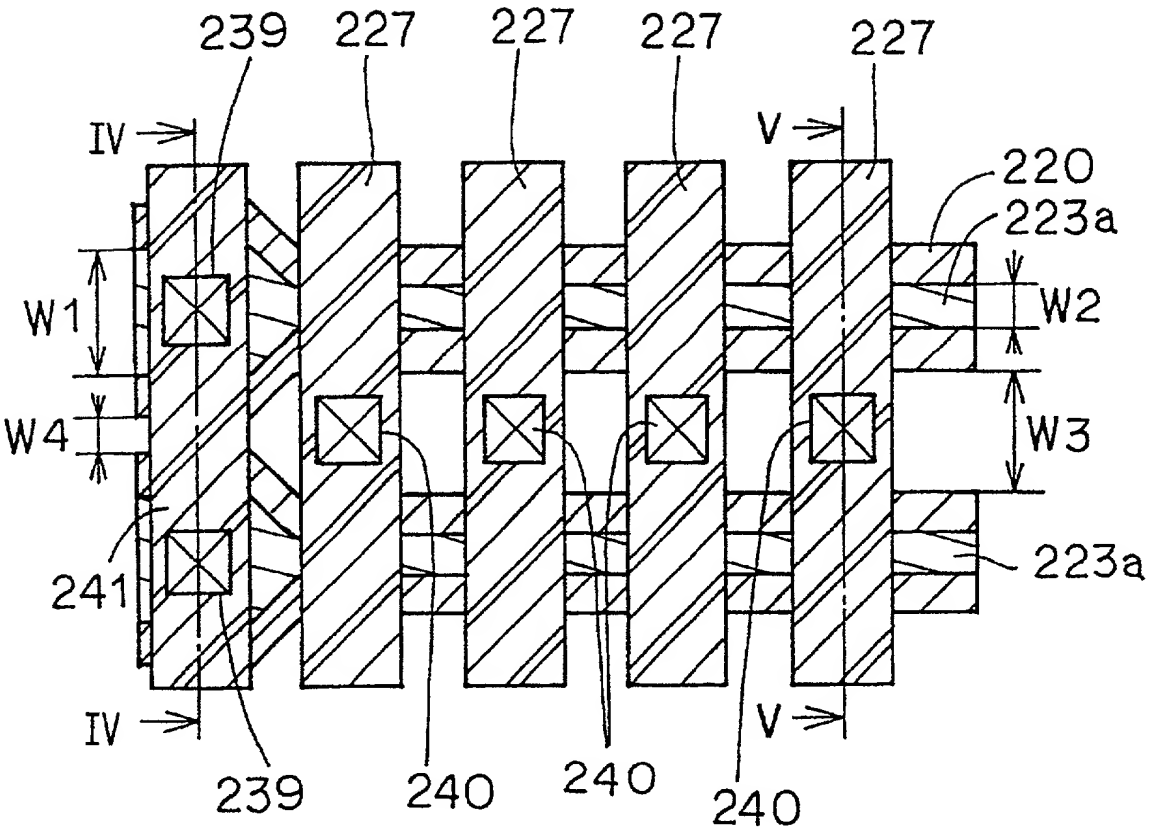


FIG. 101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223a
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FIG. 102A

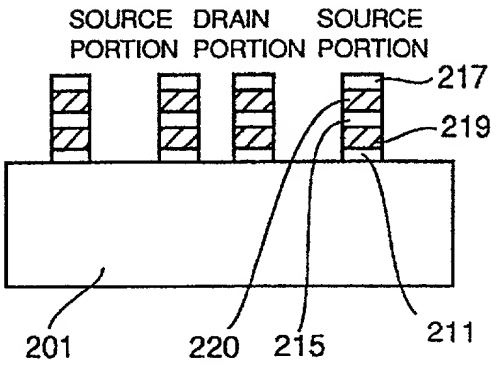


FIG. 102B

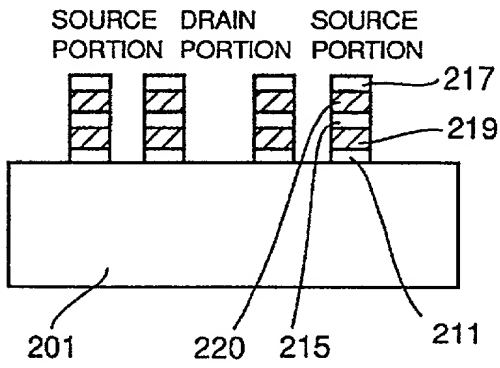


FIG. 103A

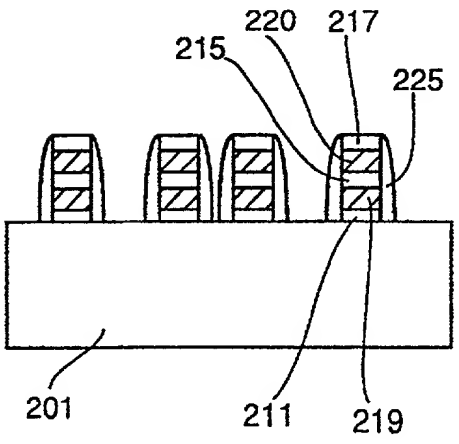


FIG. 103B

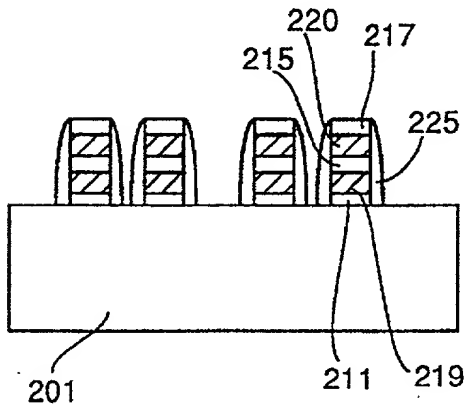


FIG. 104A

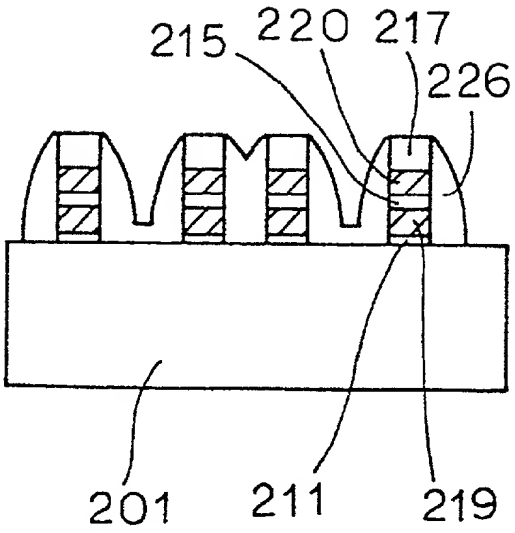


FIG. 104B

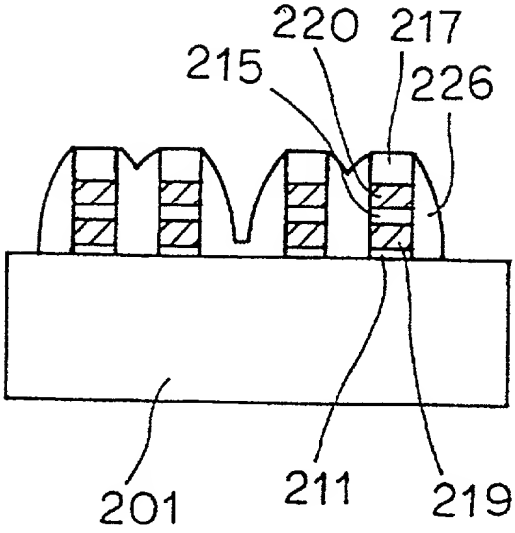


FIG. 105A

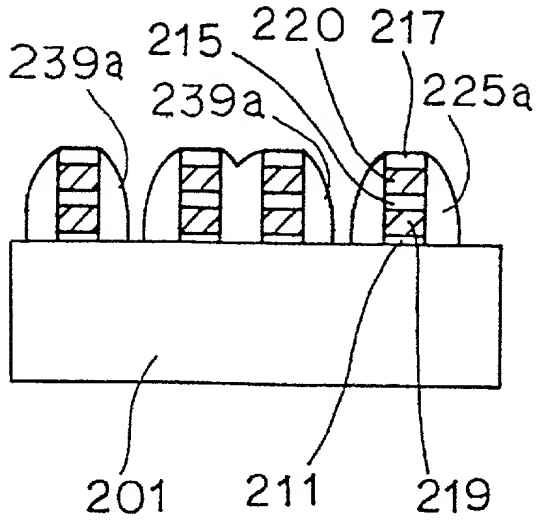


FIG. 105B

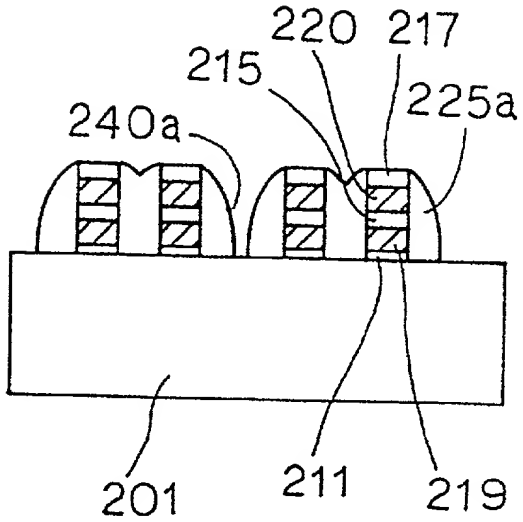


FIG. 106A

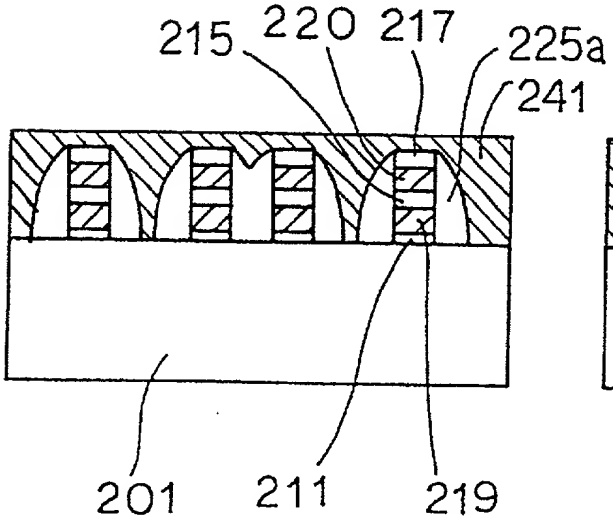


FIG. 106B

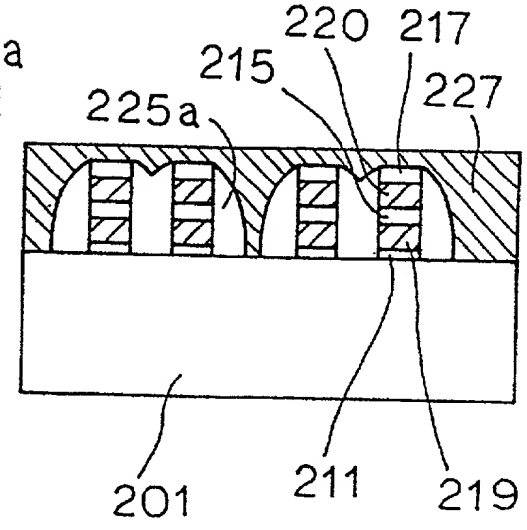


FIG. 107A

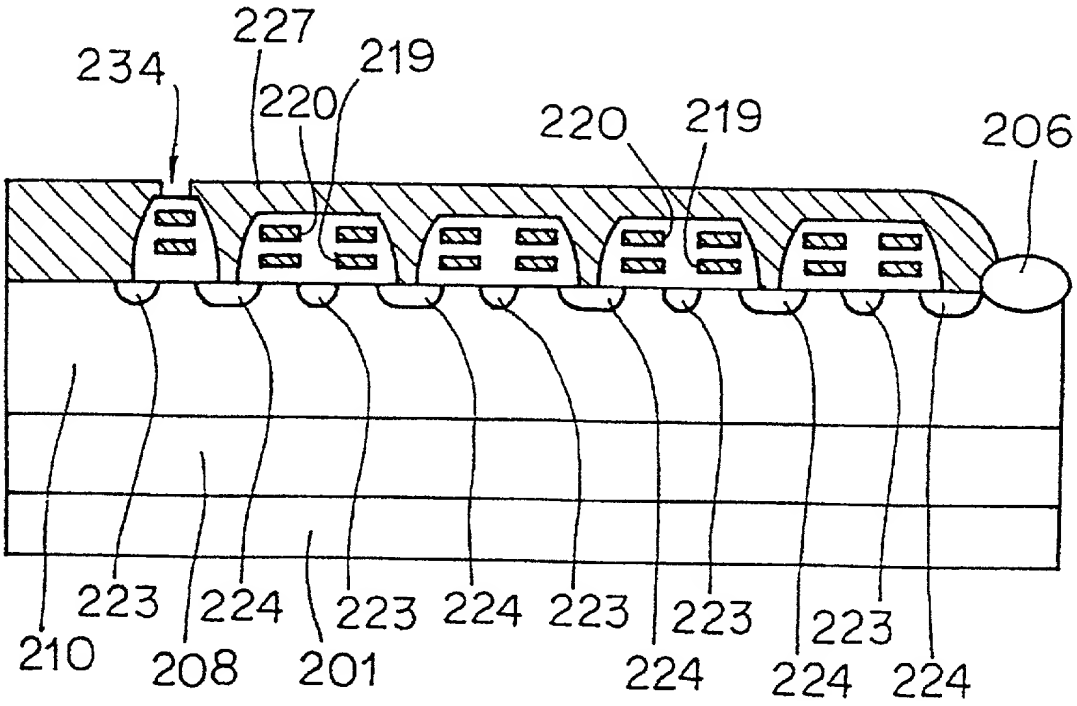
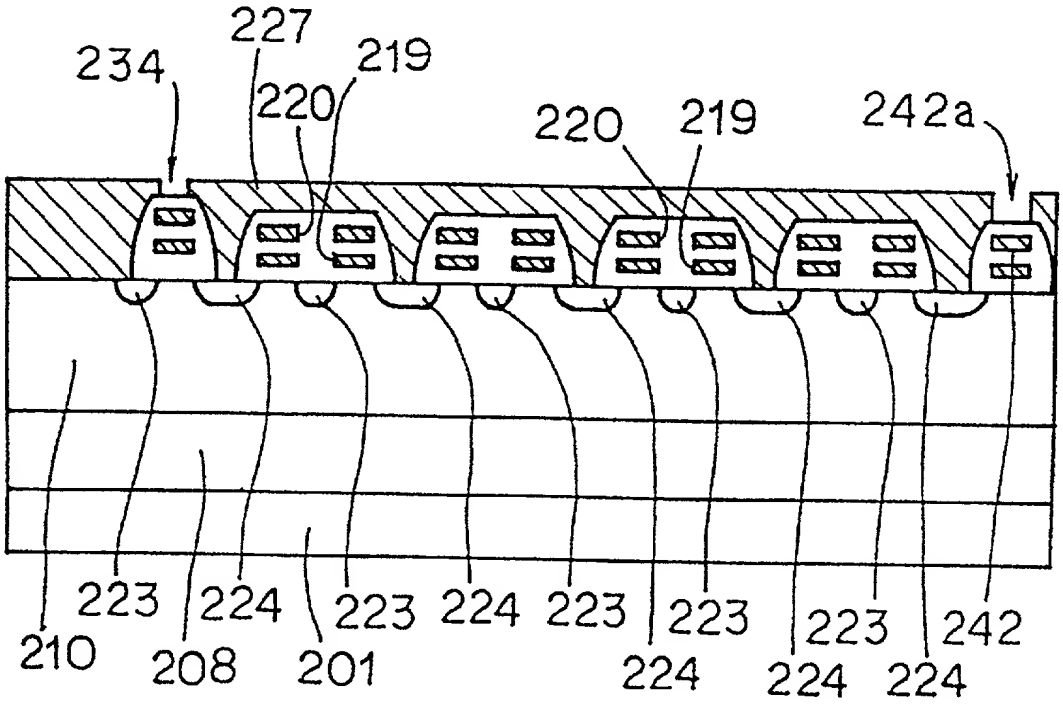


FIG. 107B



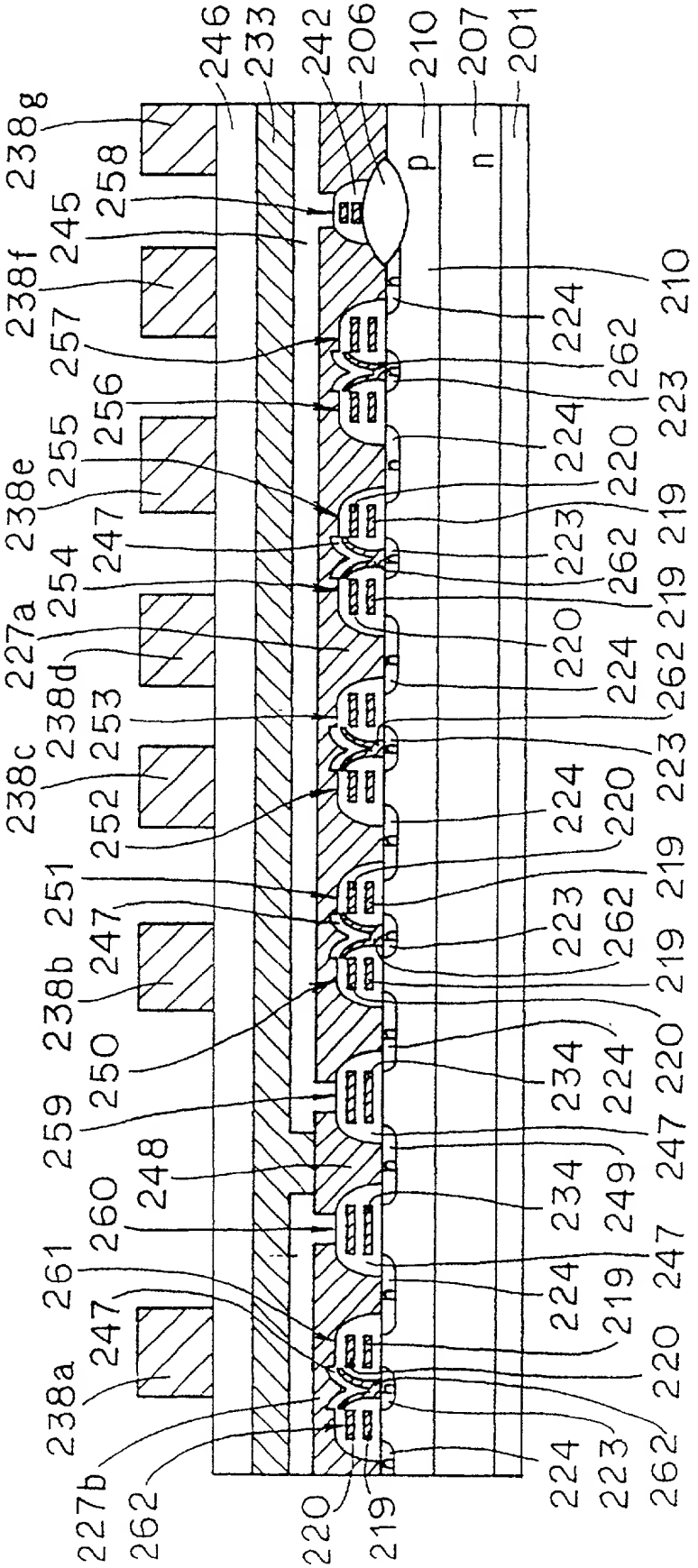

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FIG. 108

FIG. 109

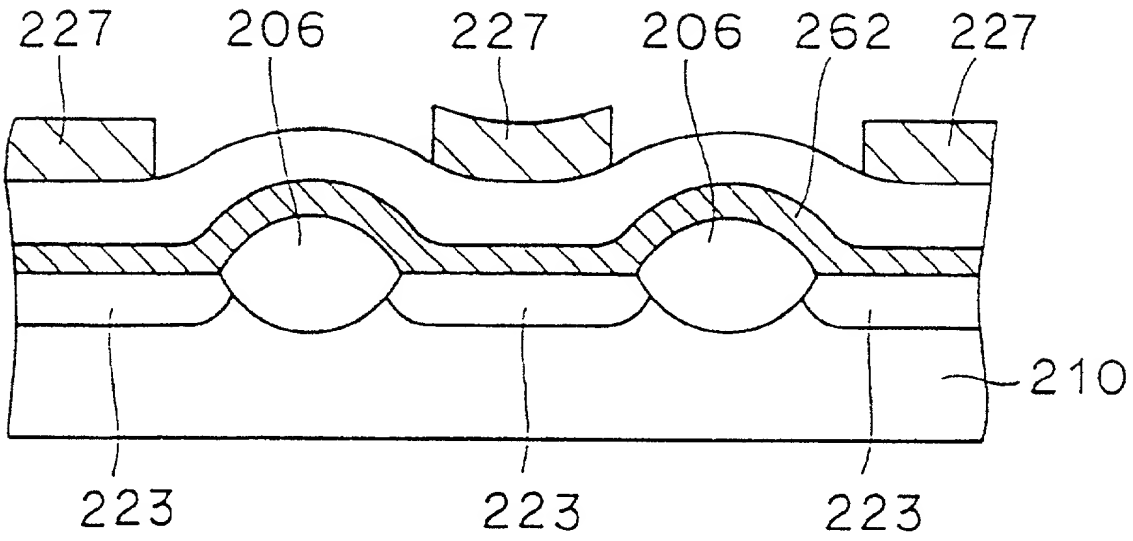


FIG. 110

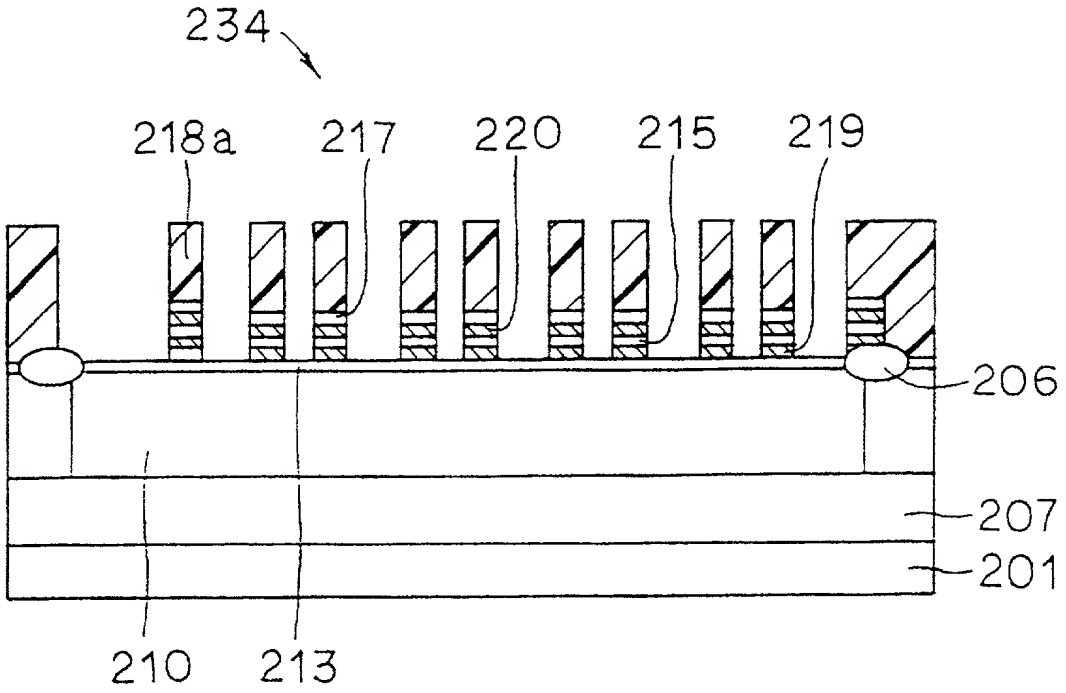


FIG. 111

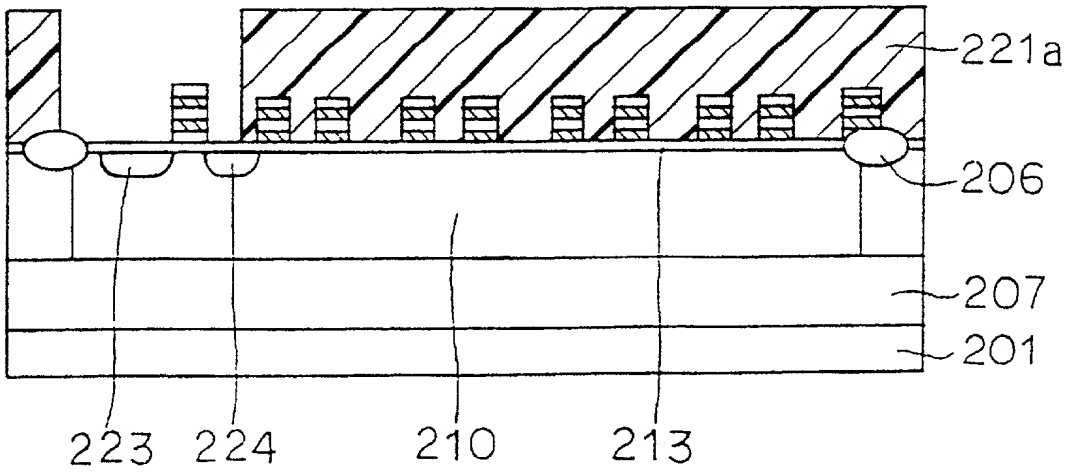


FIG. 112

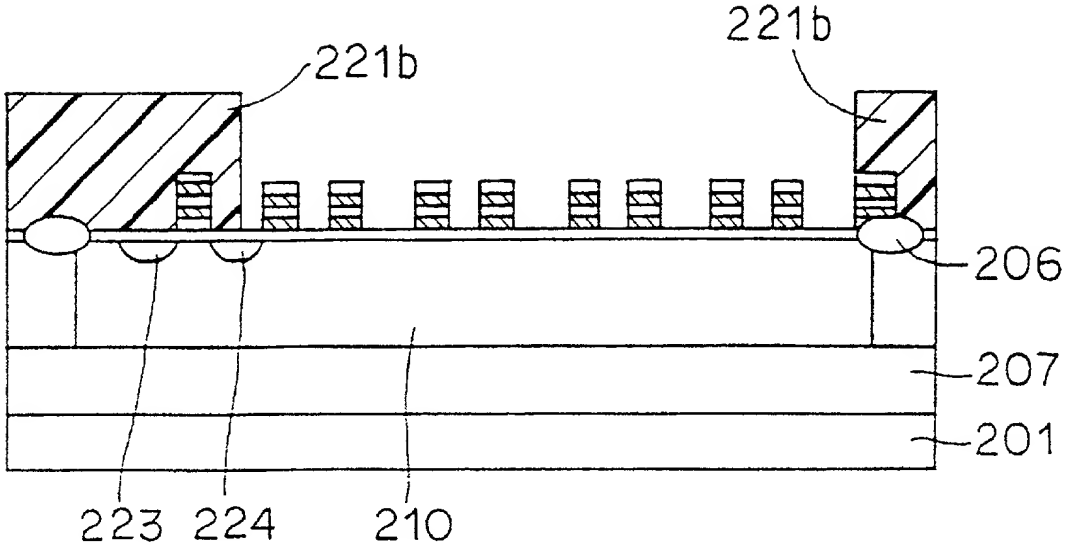


FIG. 113

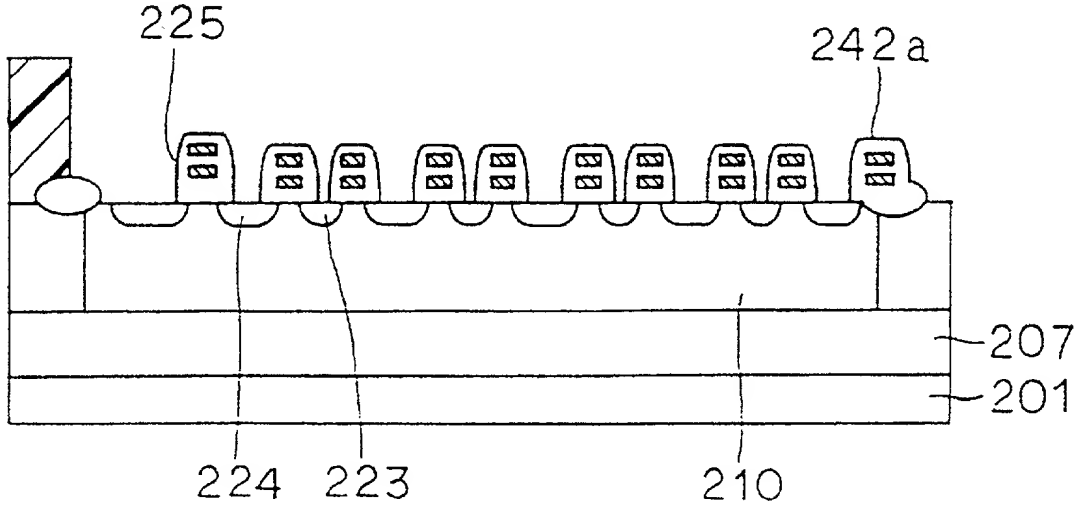


FIG. 114

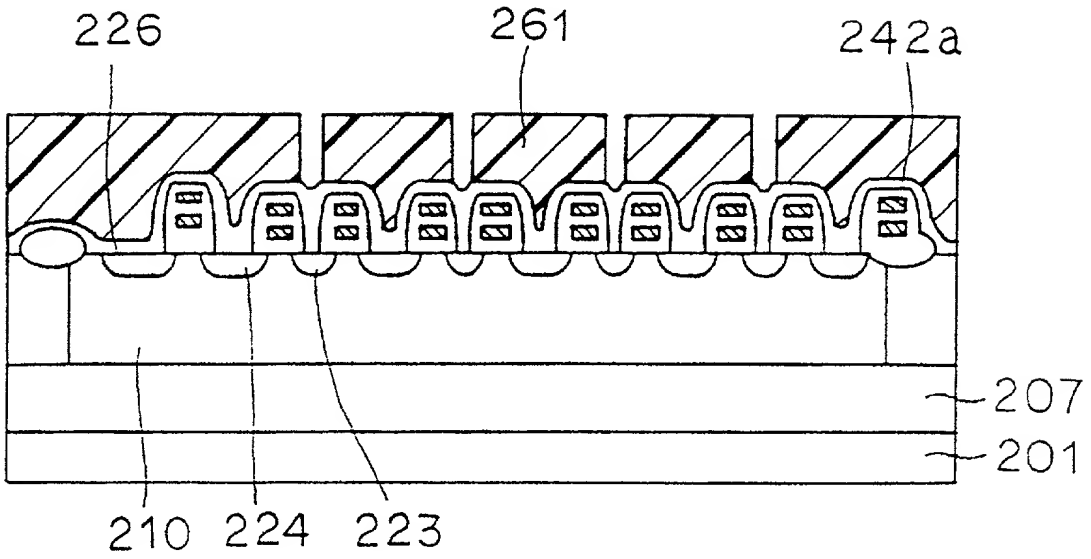


FIG. 115

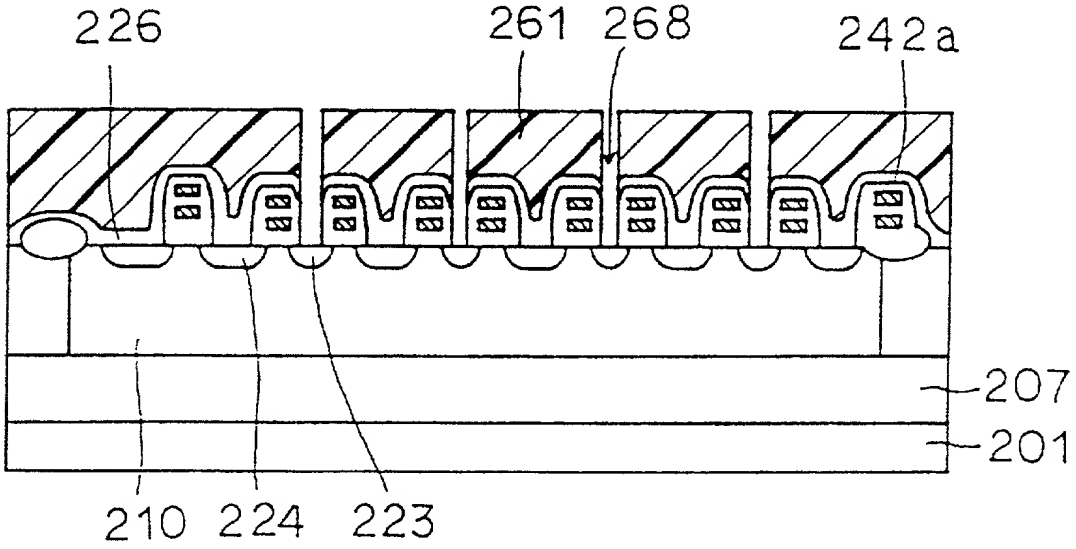


FIG. 116

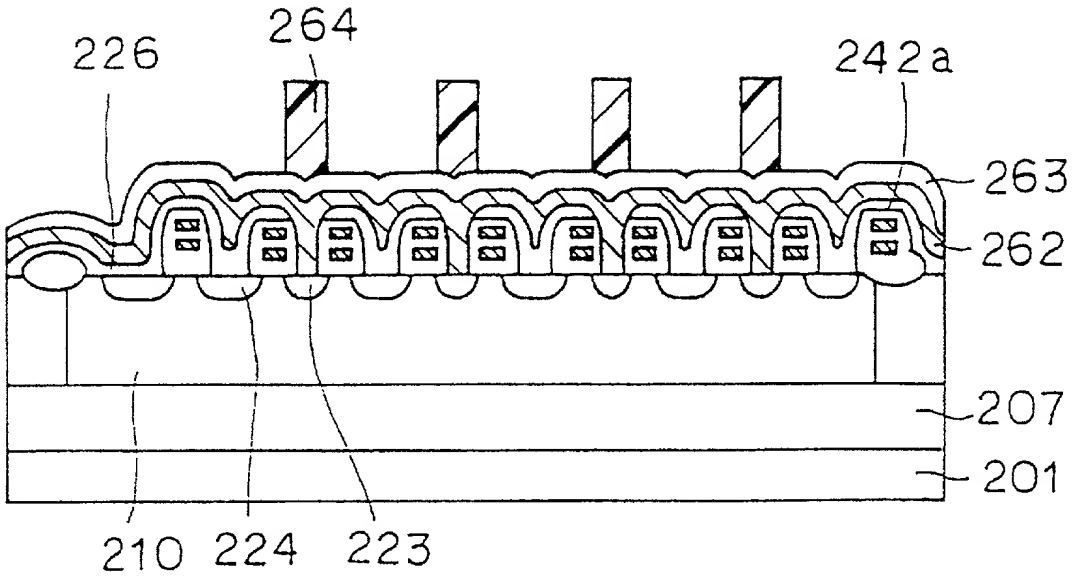


FIG. 117

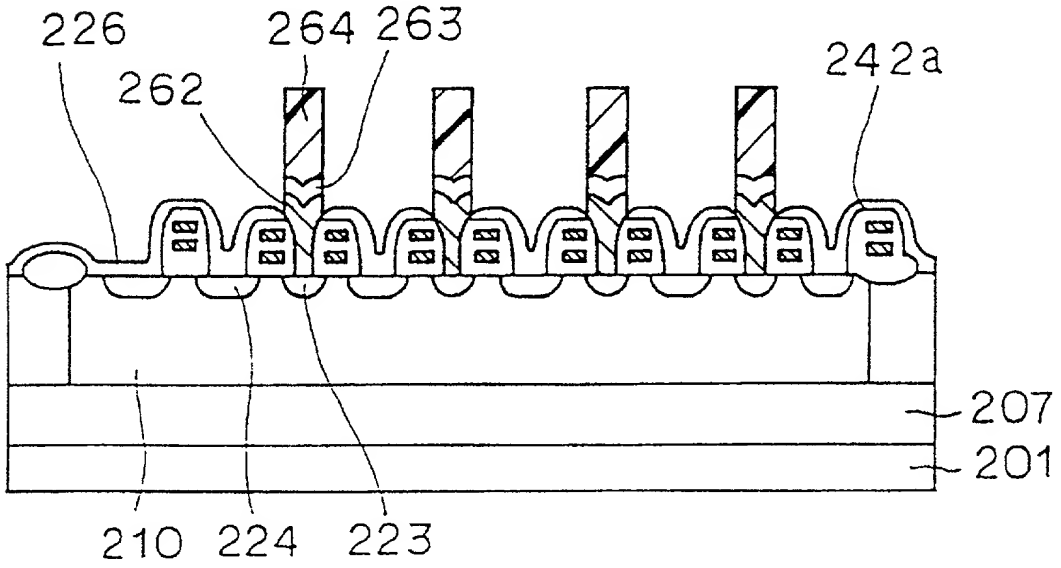


FIG. 118

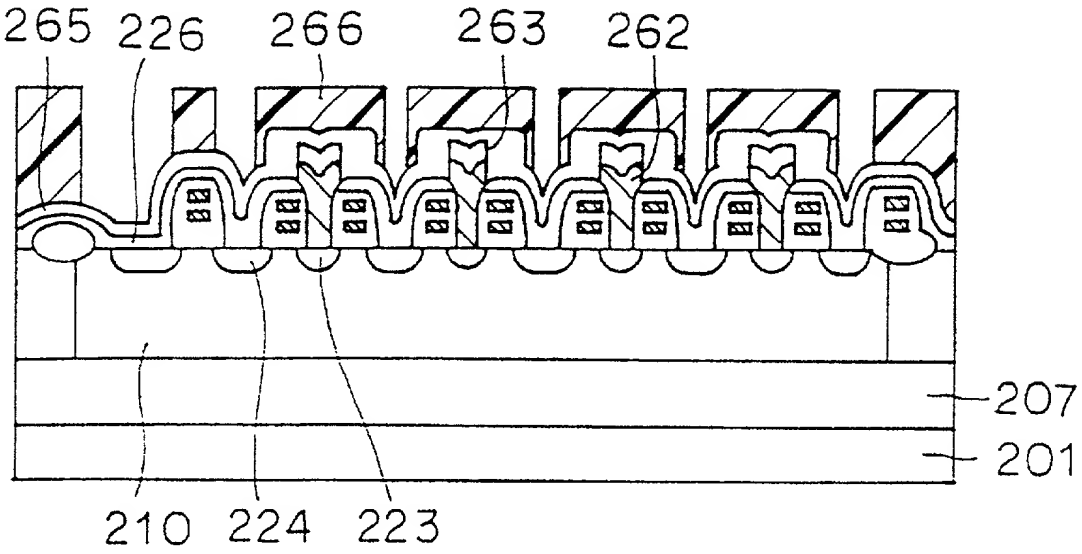


FIG. 119

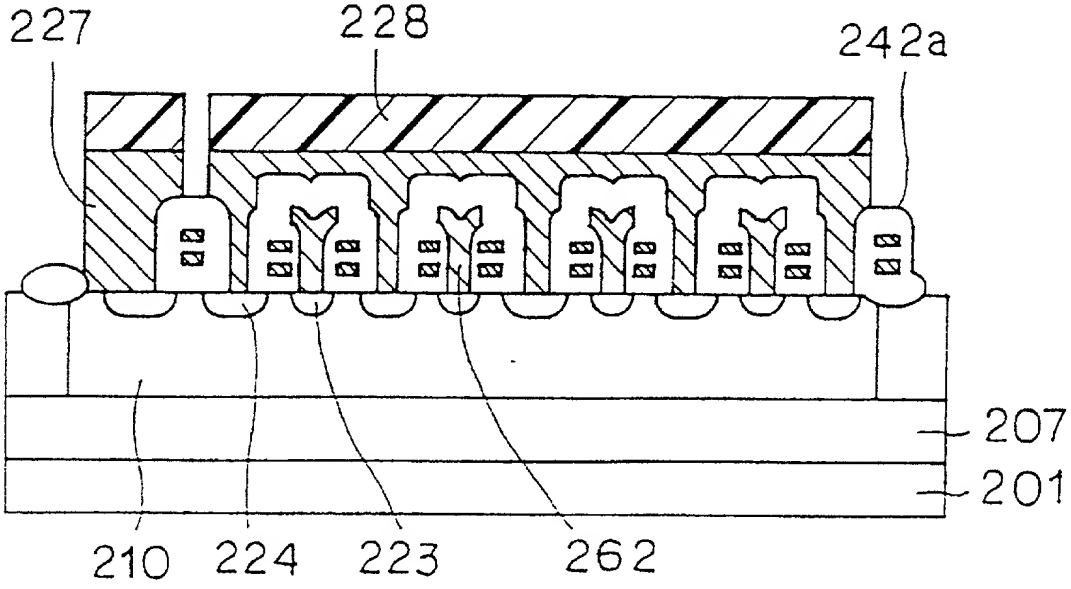


FIG. 120

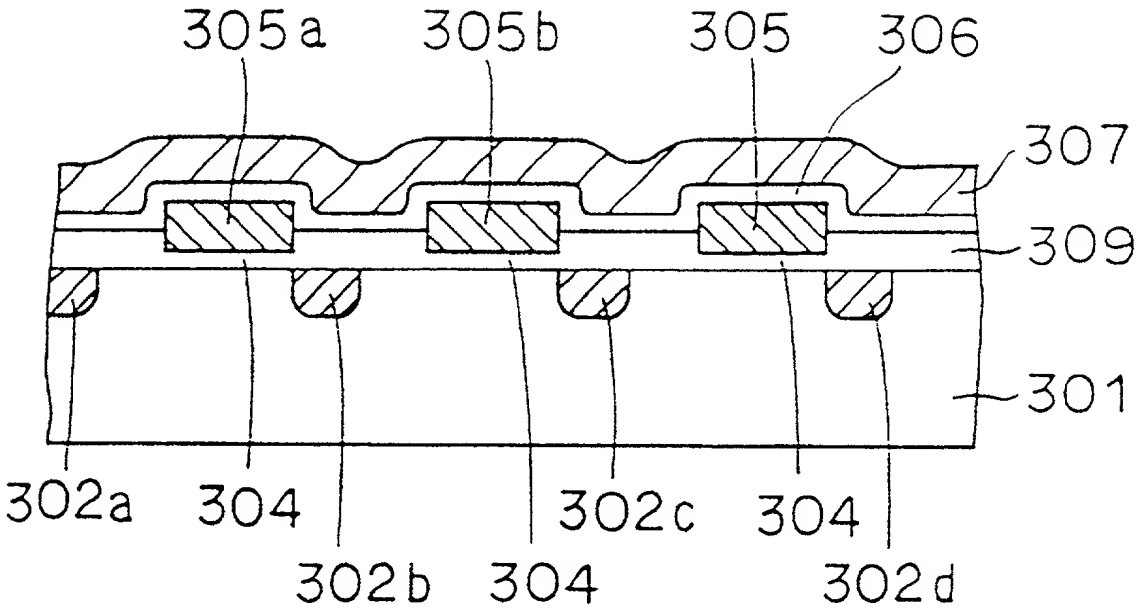


FIG. 121A

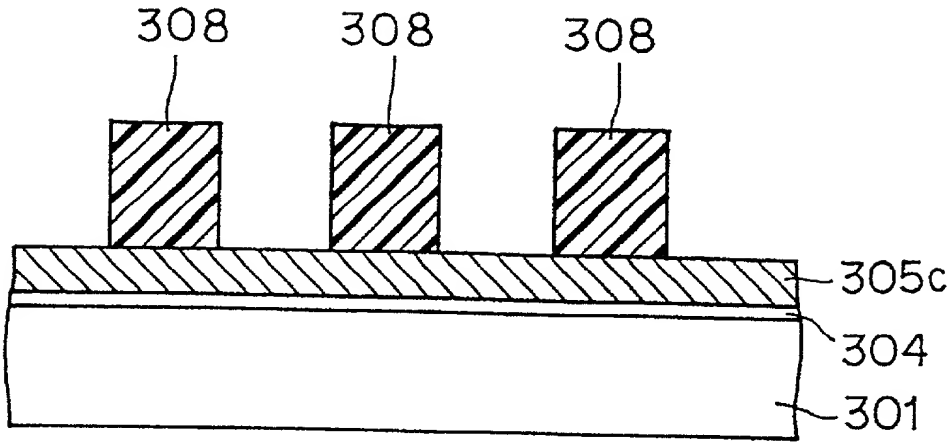


FIG. 121B

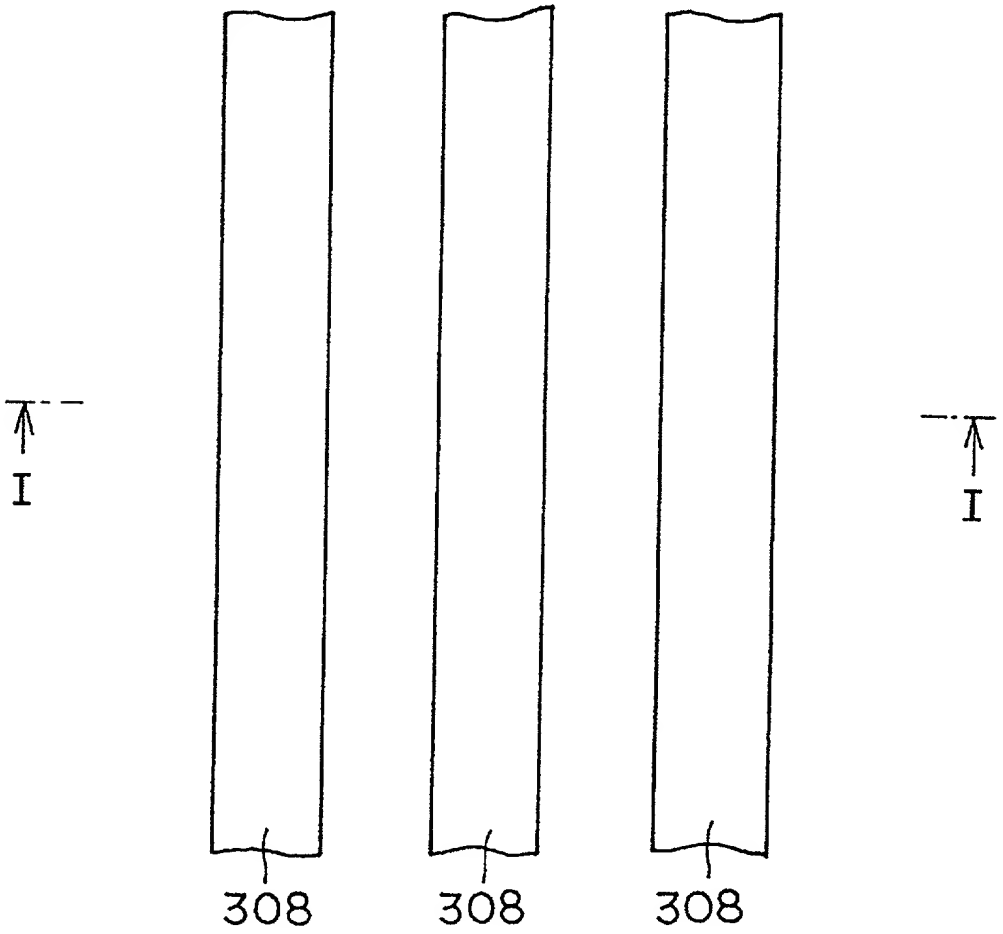


FIG. 122A

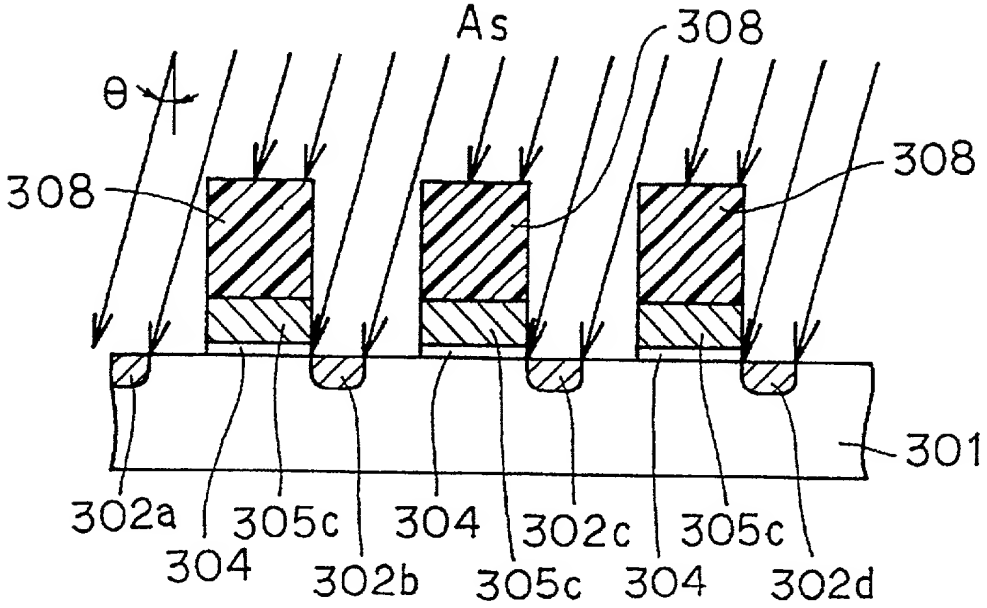


FIG. 122B

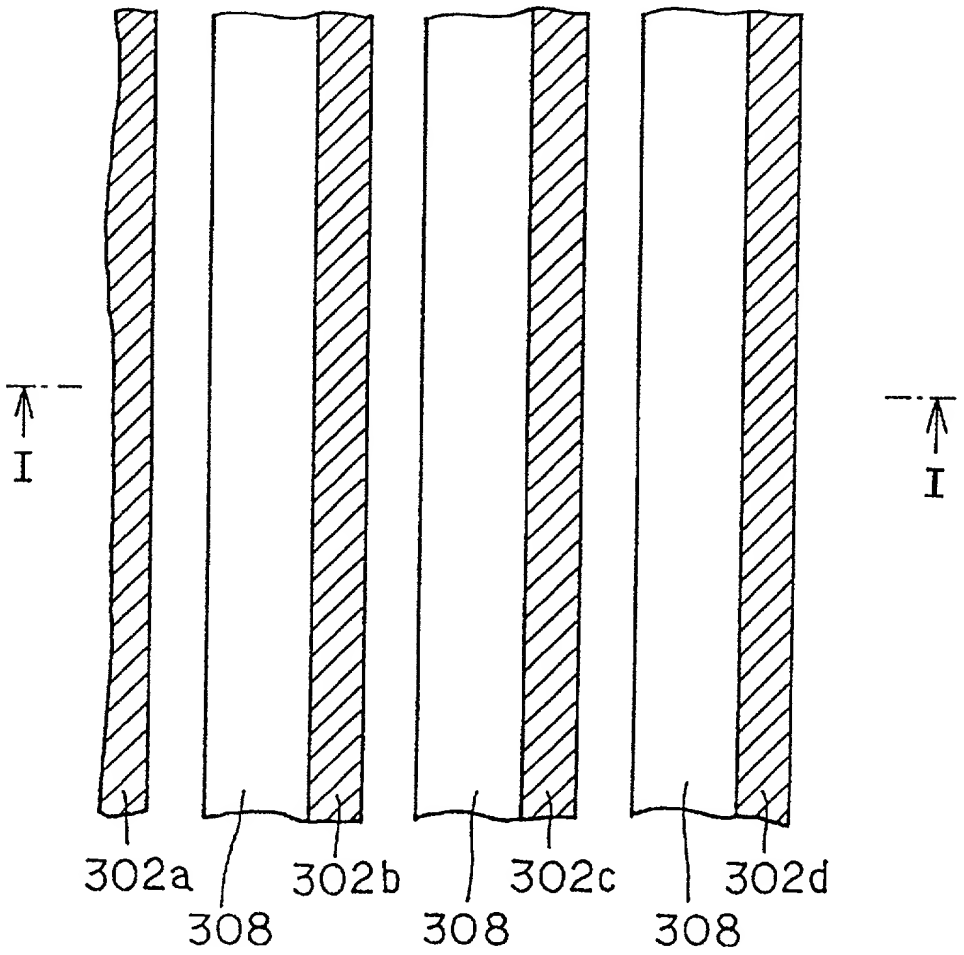


FIG. 123

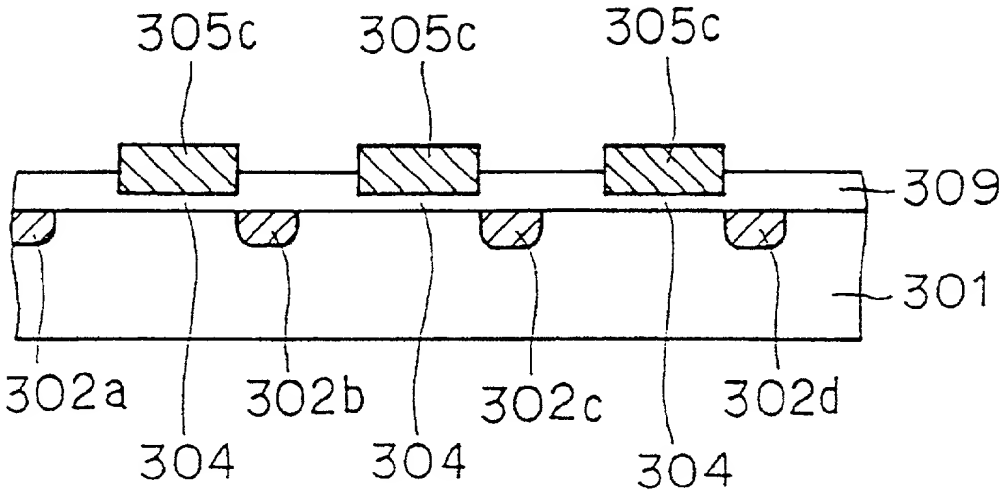


FIG. 124

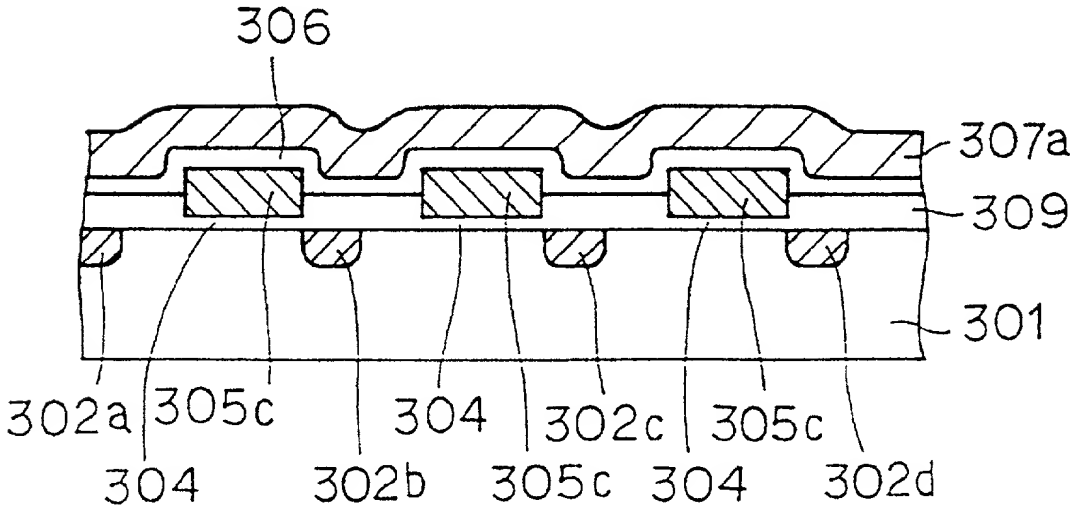


FIG. 125A

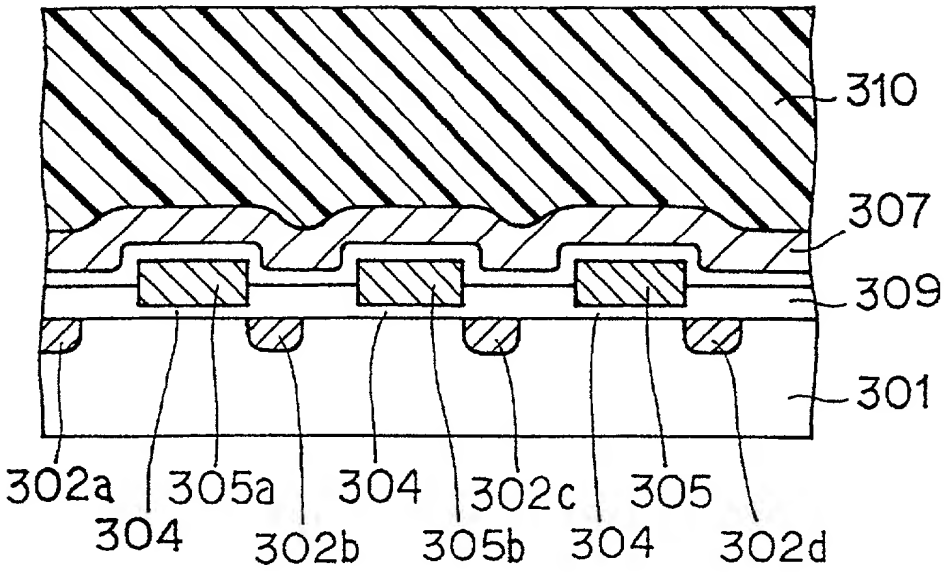


FIG. 125B

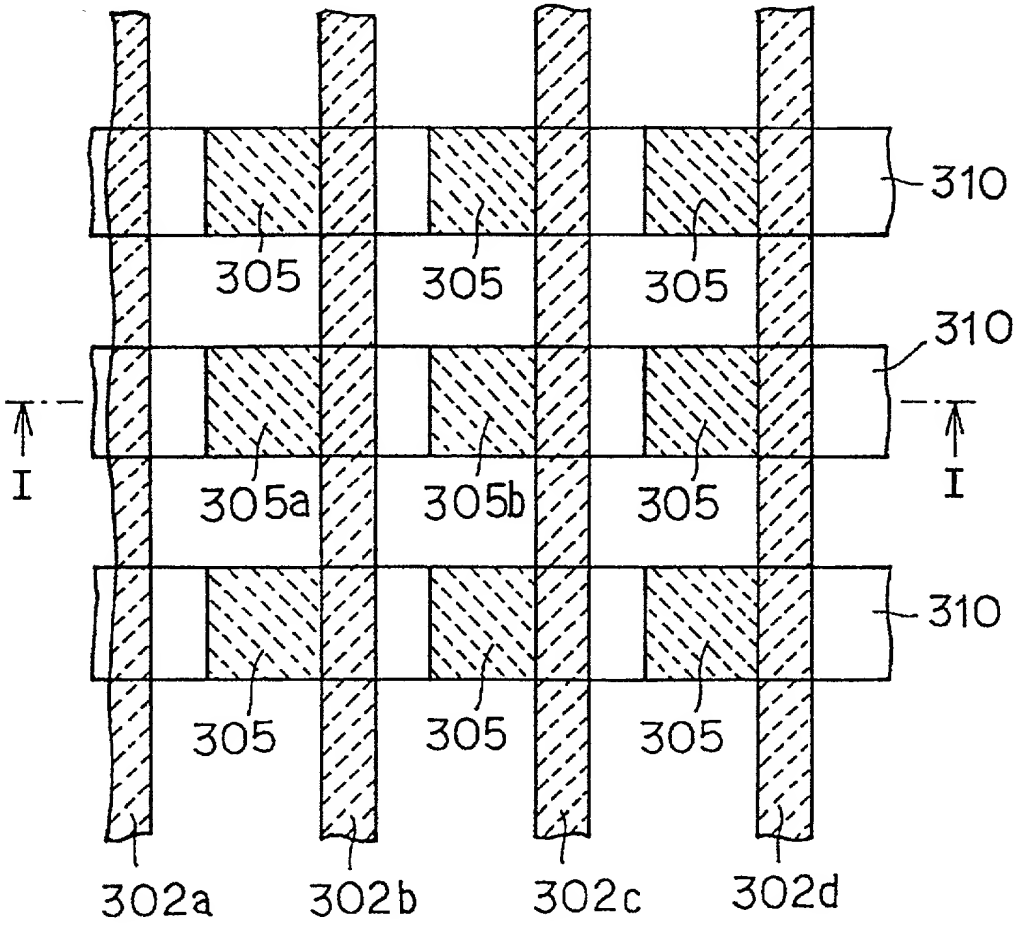


FIG. 126

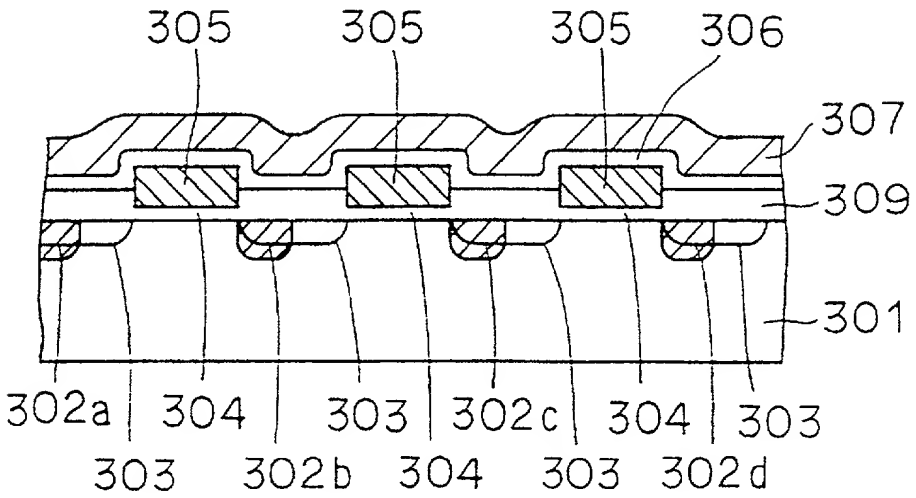


FIG. 127

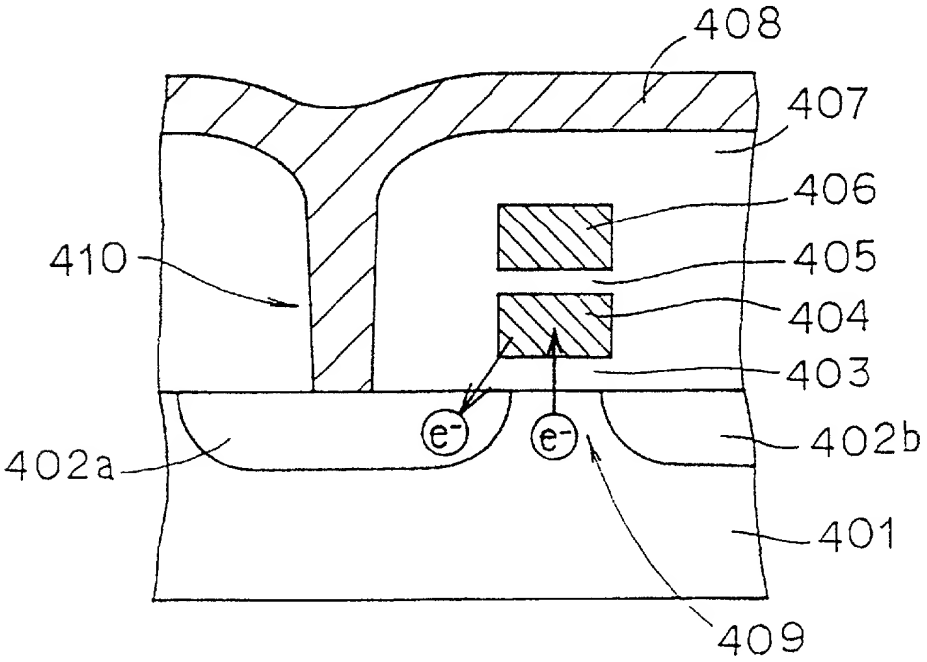


FIG. 128 PRIOR ART

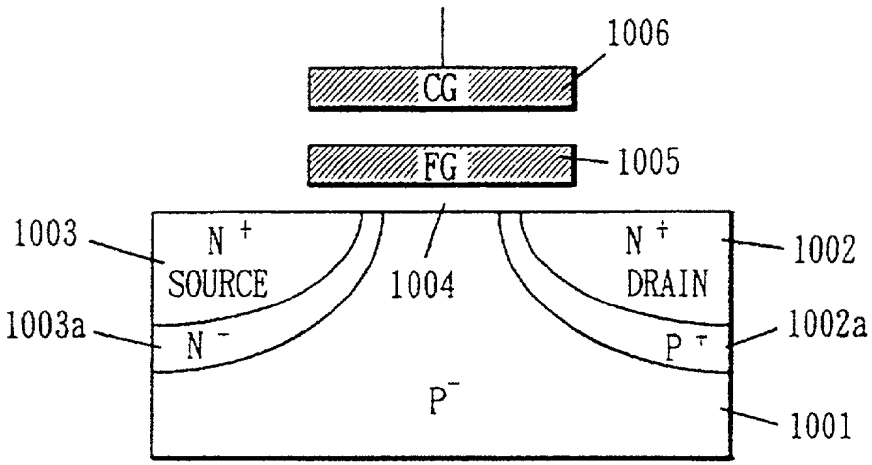


FIG. 129 PRIOR ART

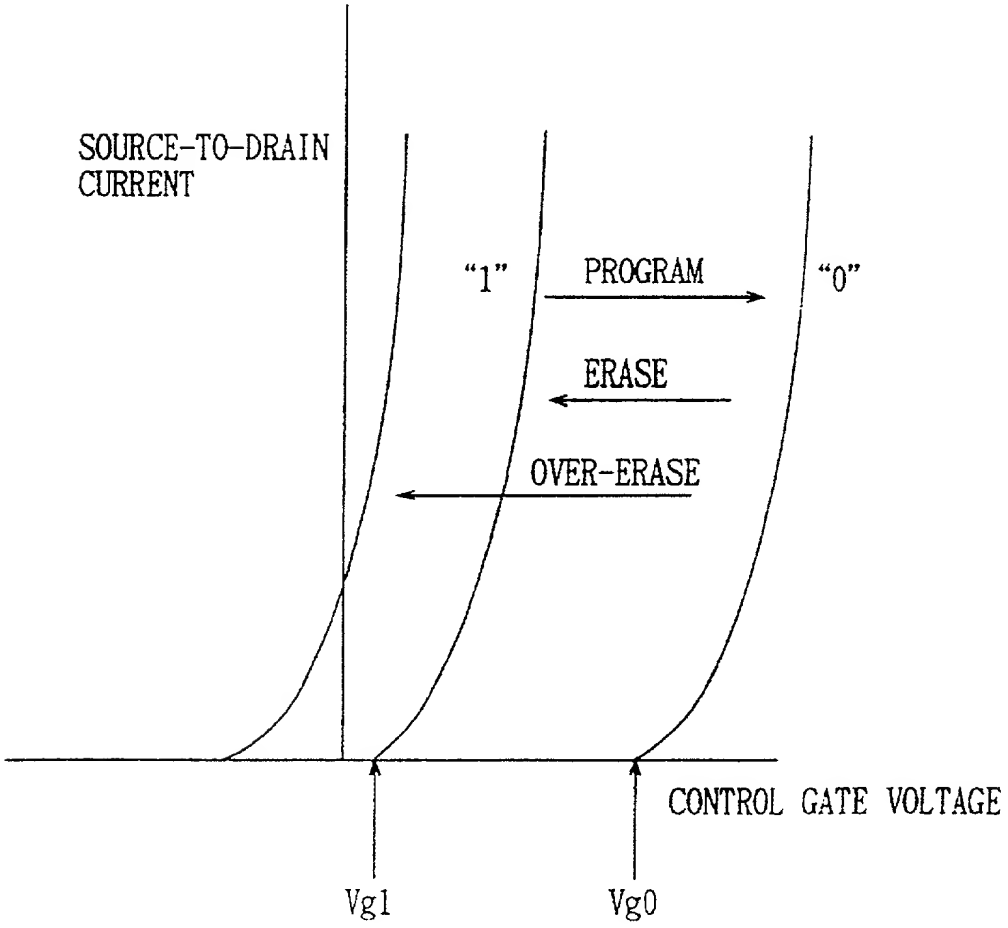


FIG. 130A

PRIOR ART

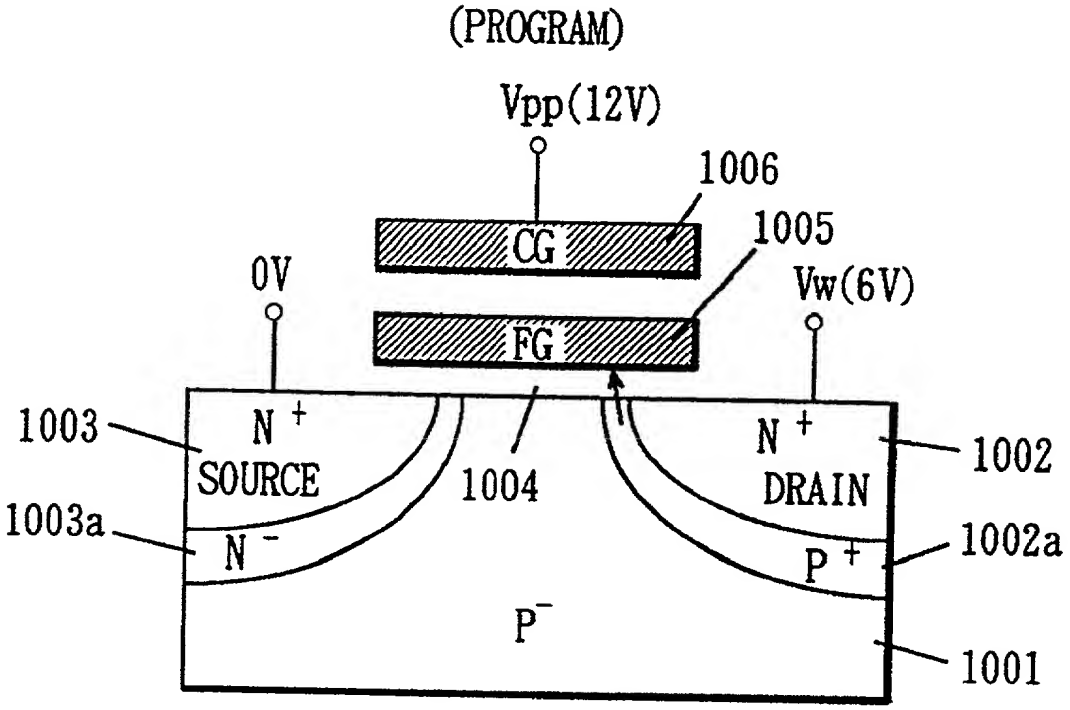


FIG. 130B

PRIOR ART

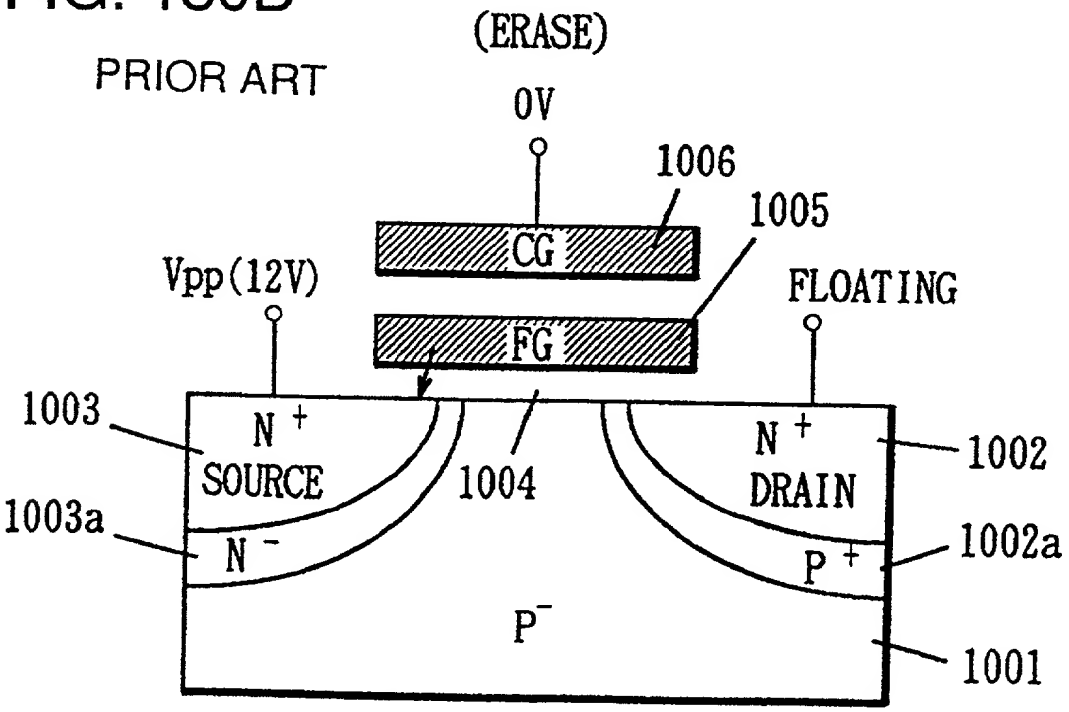


FIG. 131 PRIOR ART

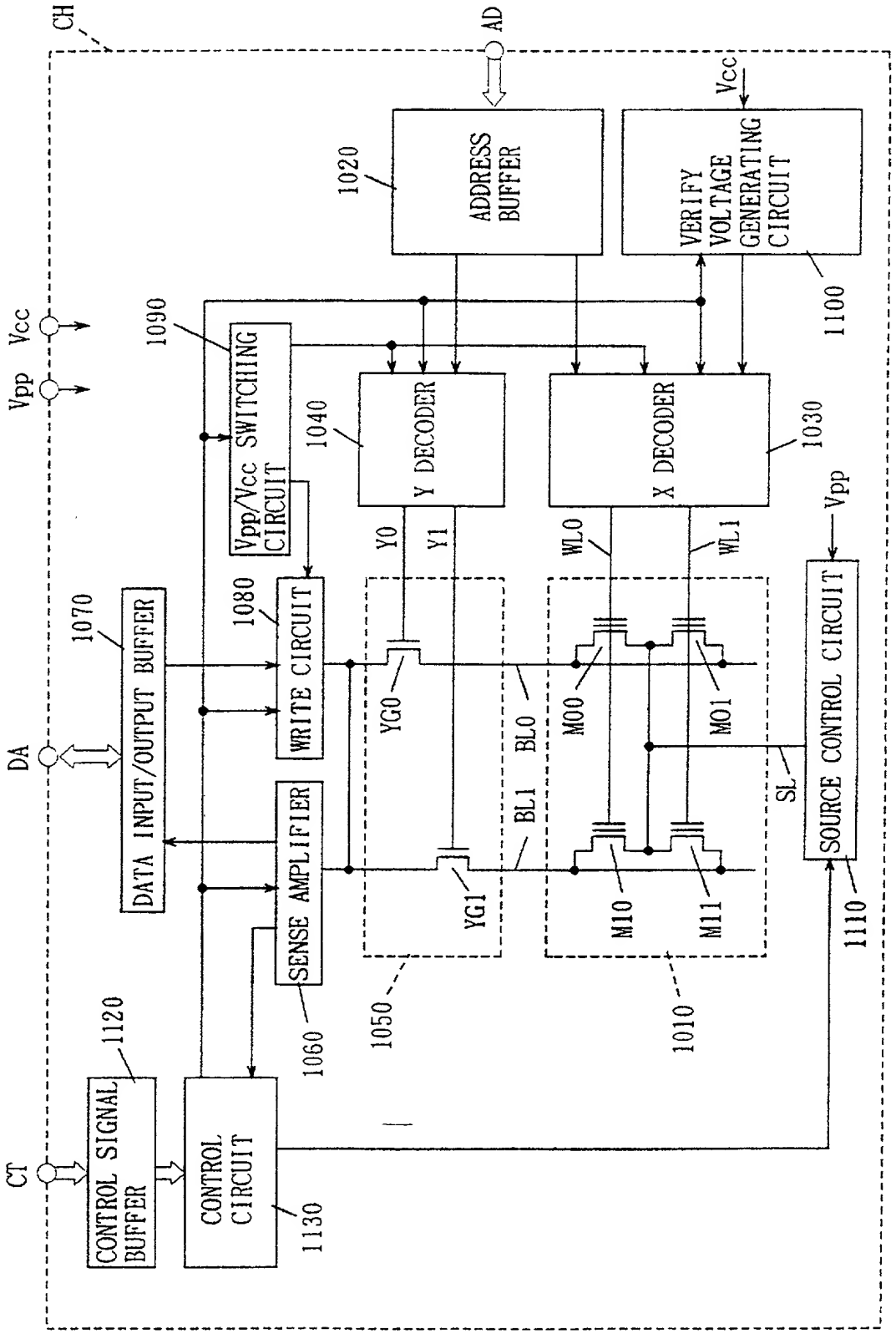


FIG. 132 PRIOR ART

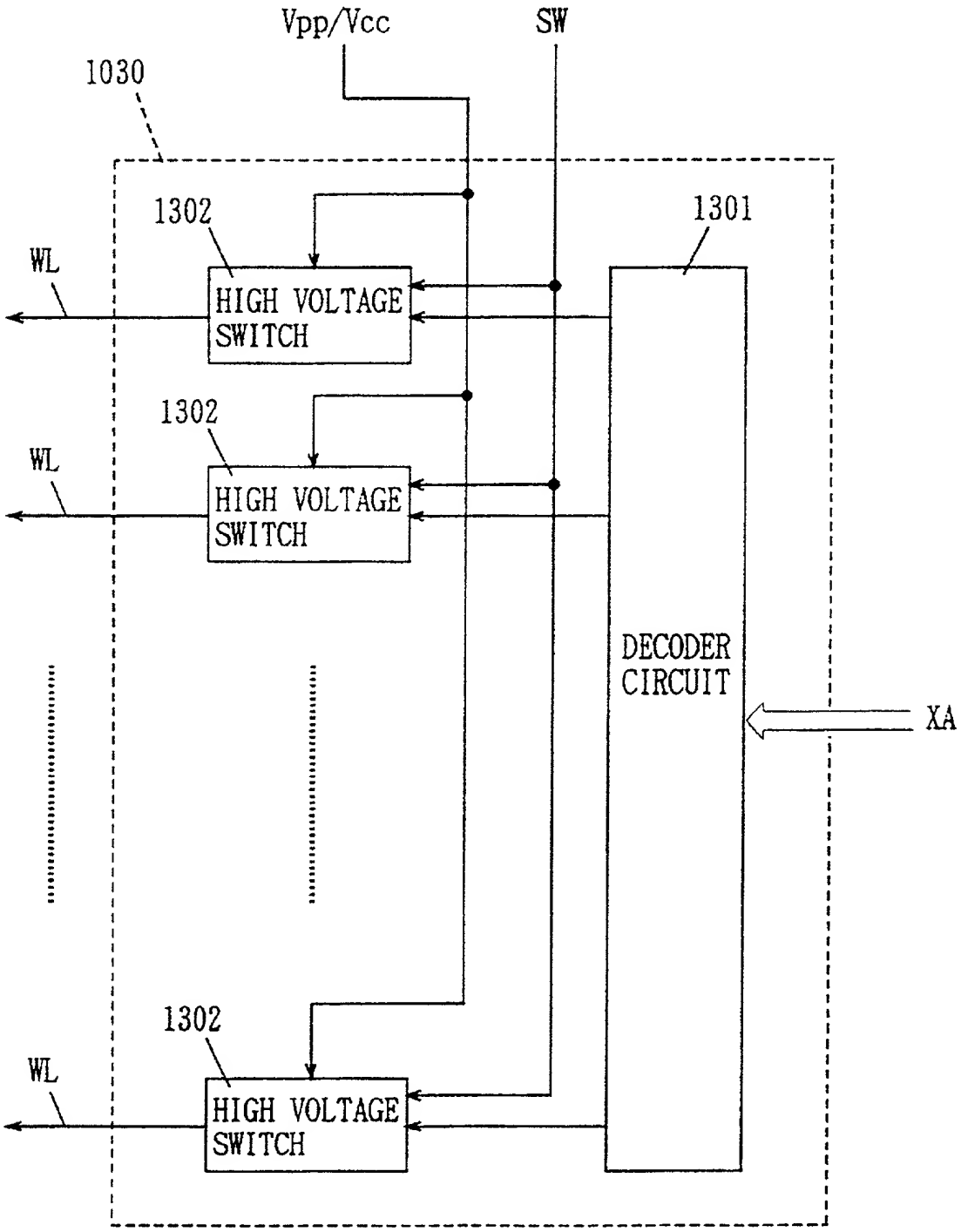


FIG. 133 PRIOR ART

(PROGRAM OPERATION)

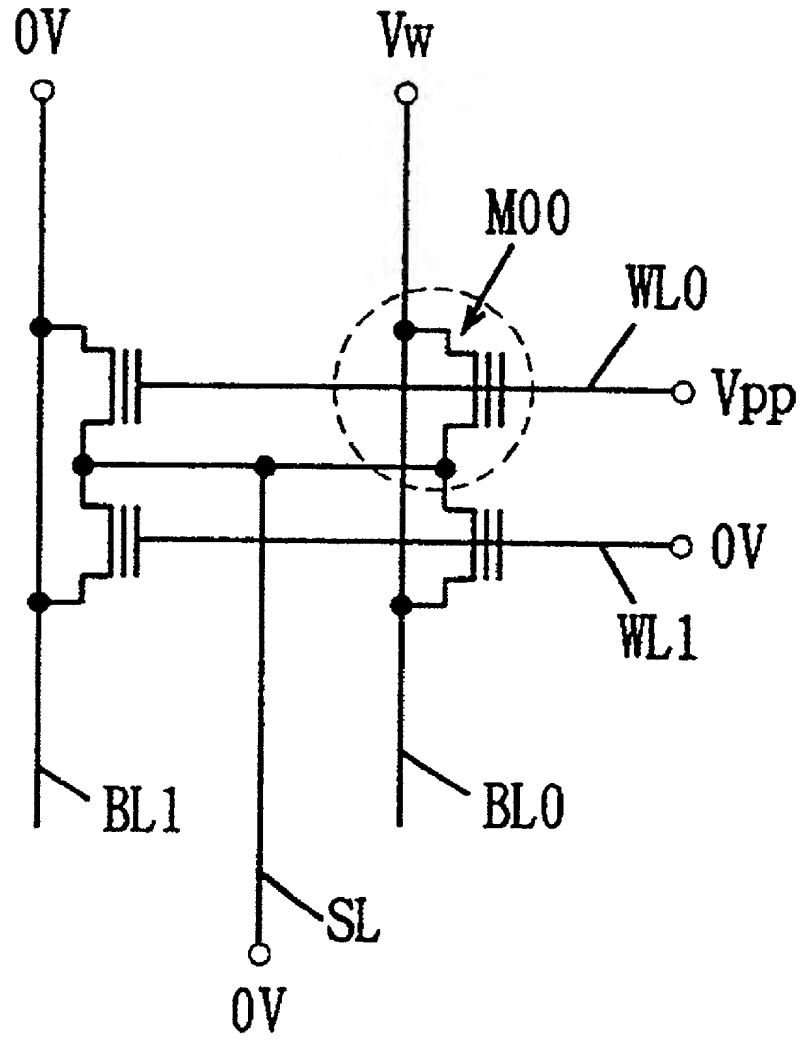


FIG. 134 PRIOR ART

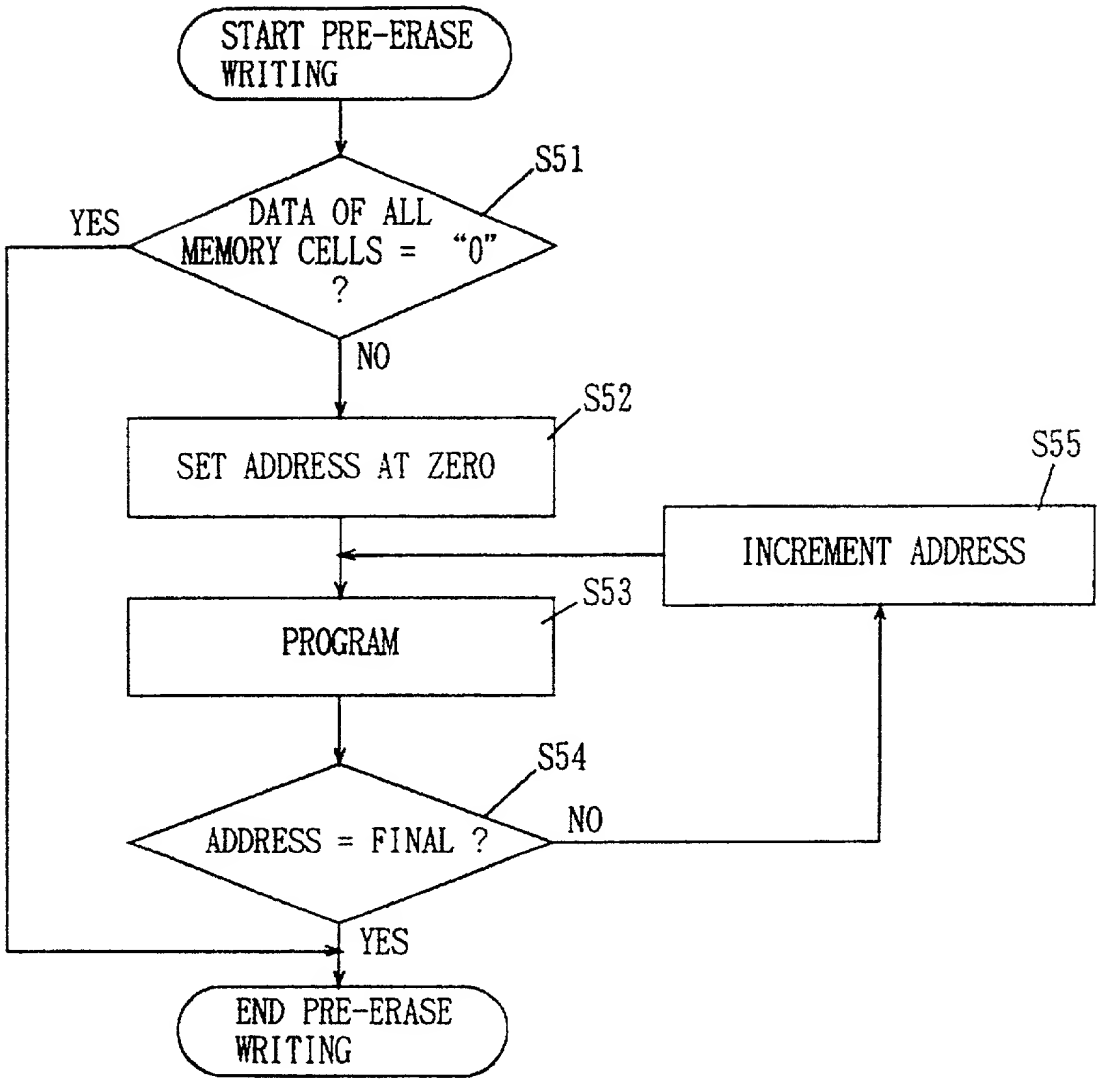


FIG. 135 PRIOR ART

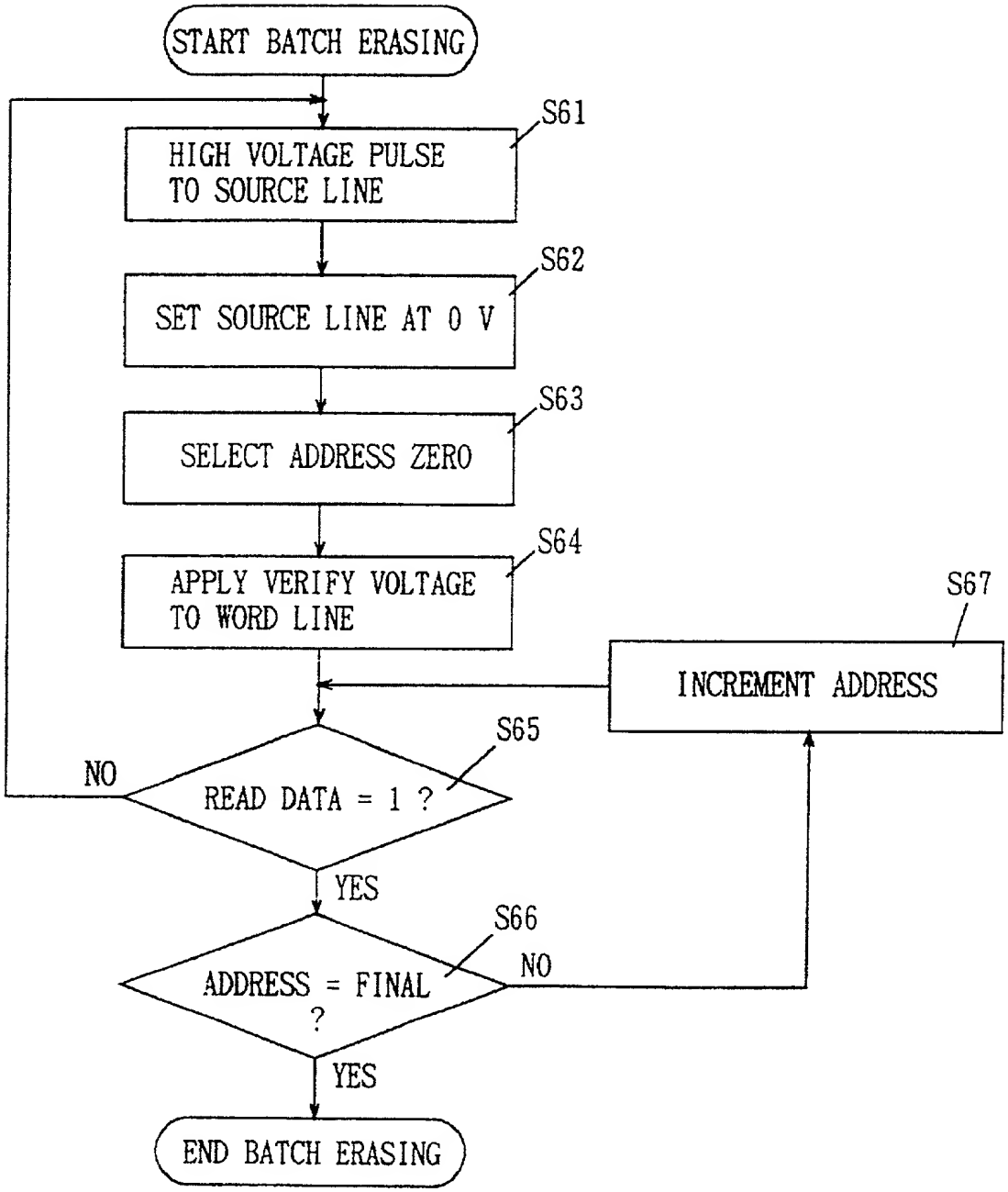


FIG. 136 PRIOR ART

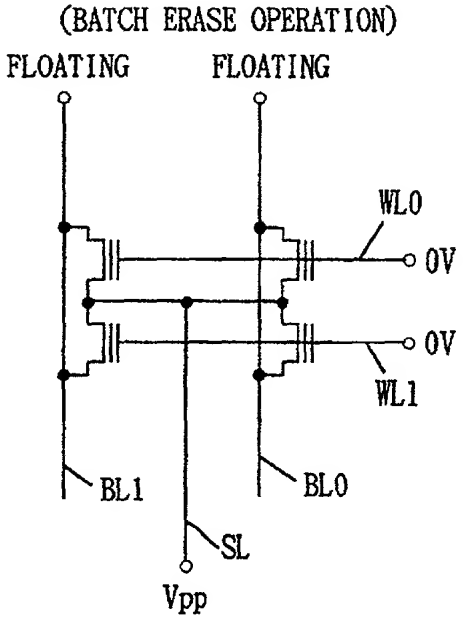
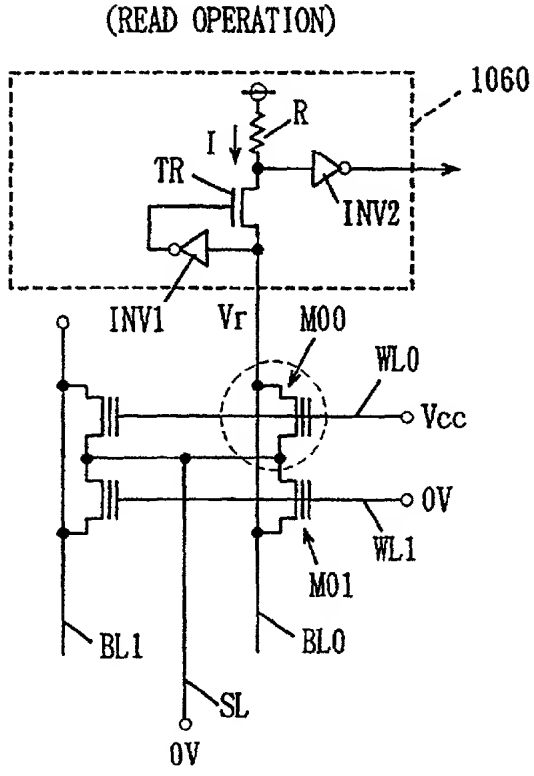


FIG. 137 PRIOR ART



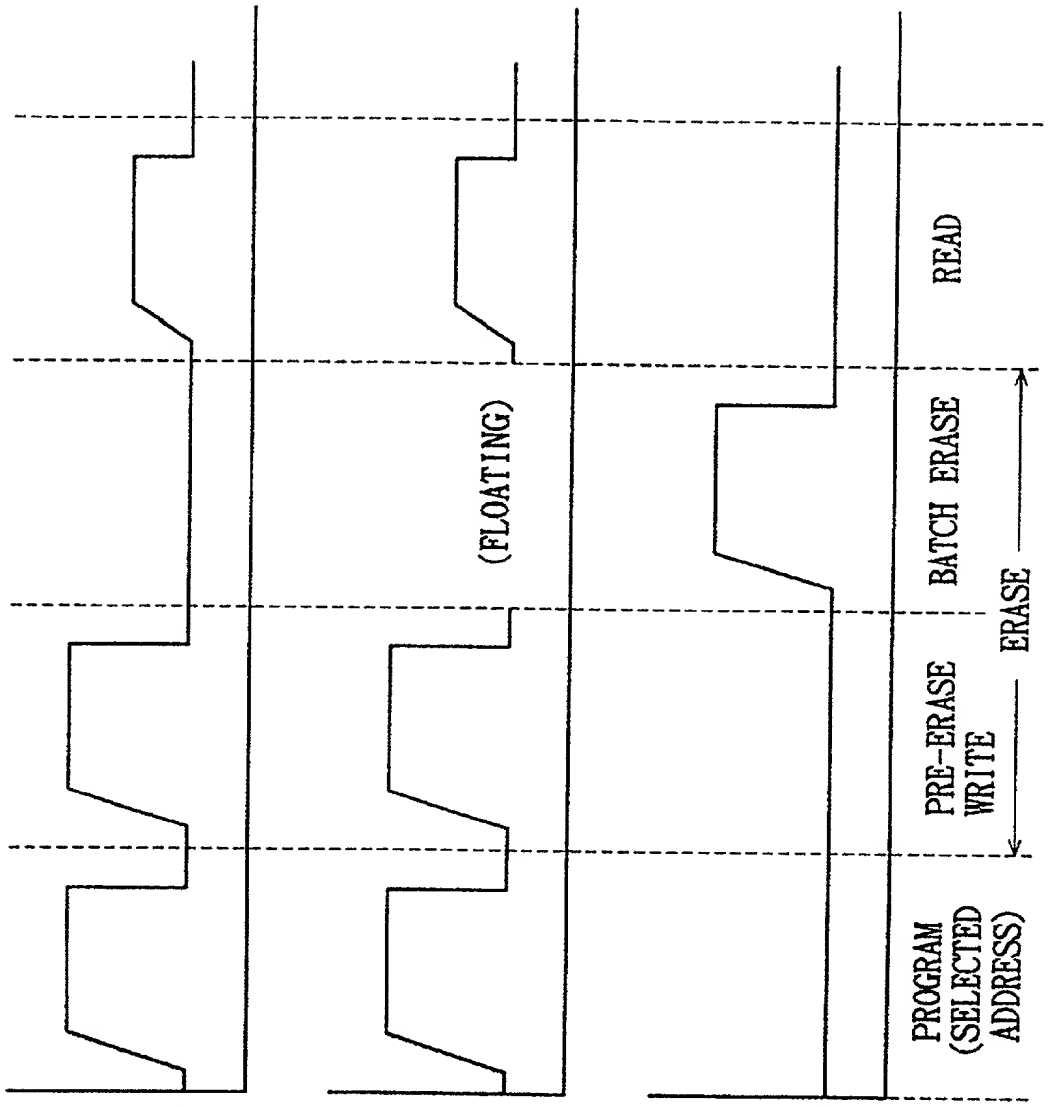


FIG. 138A

FIG. 138B

FIG. 138C

FIG. 139 PRIOR ART

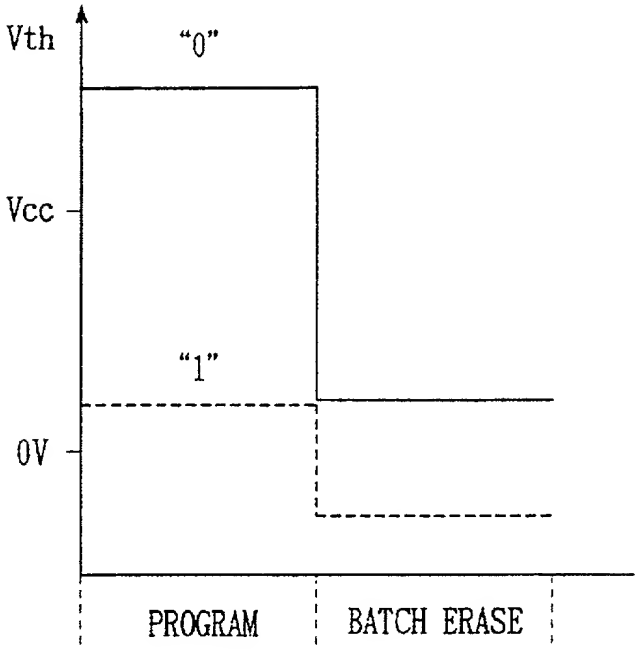


FIG. 140 PRIOR ART

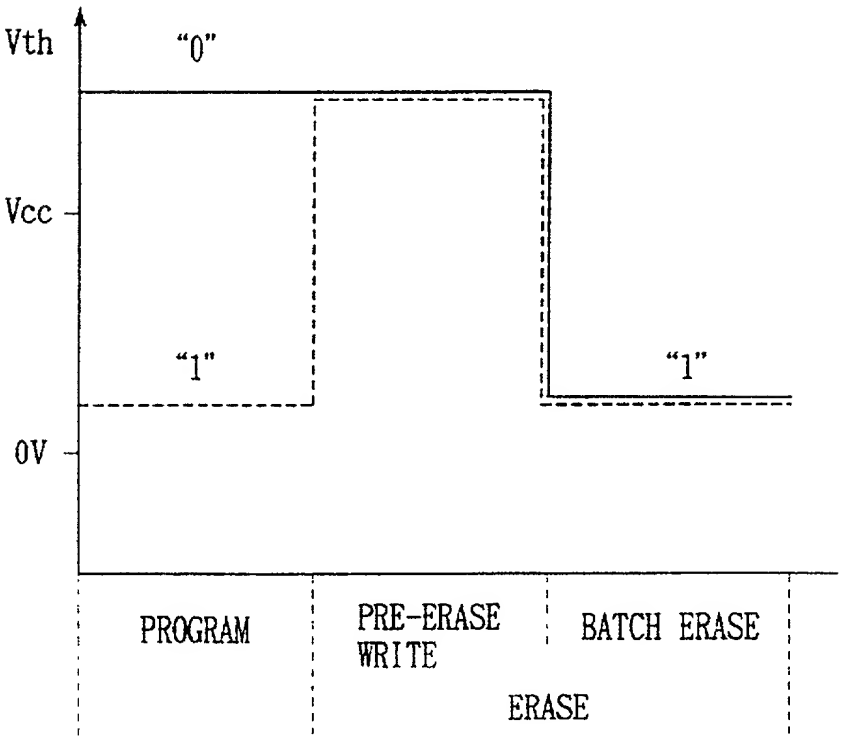


FIG. 141 PRIOR ART

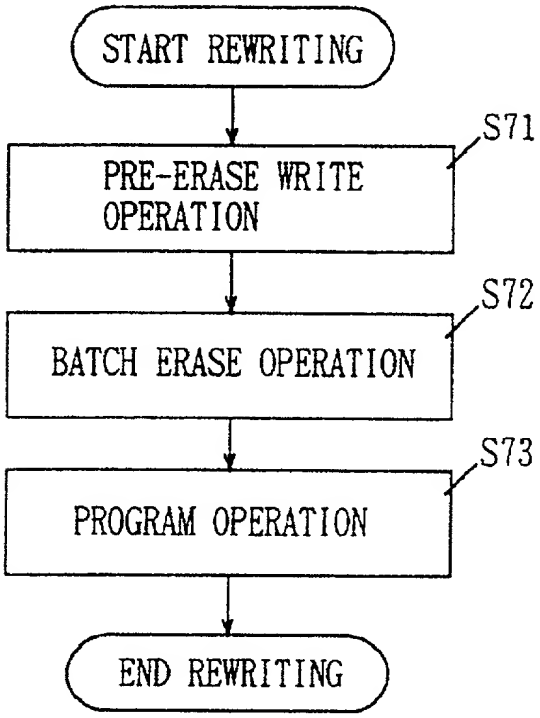


FIG. 142 PRIOR ART

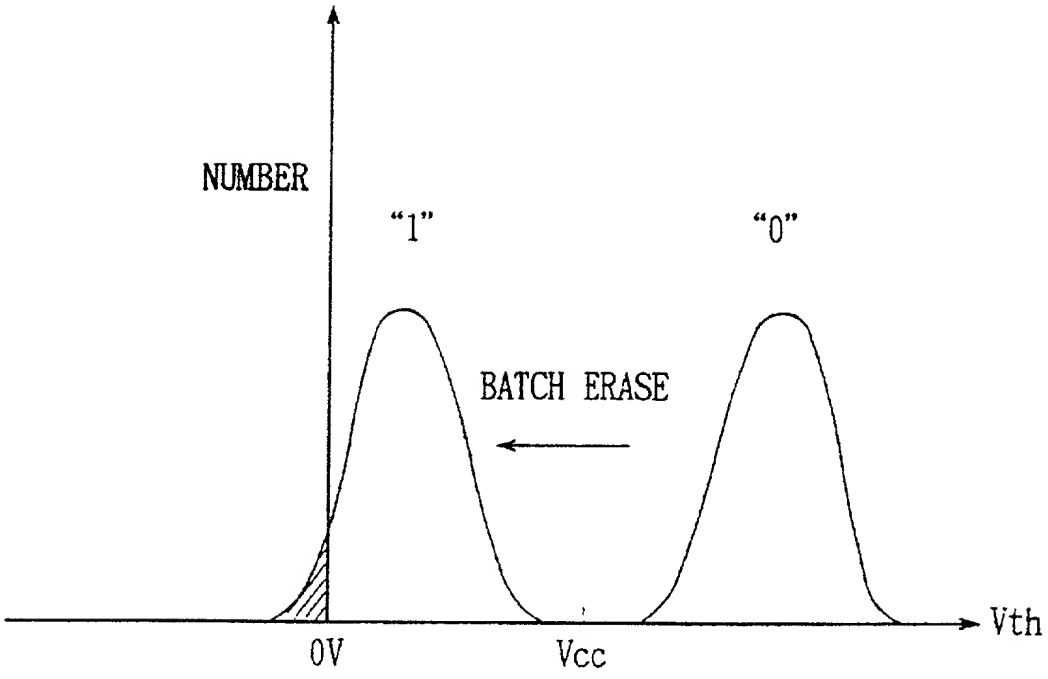


FIG. 143 PRIOR ART

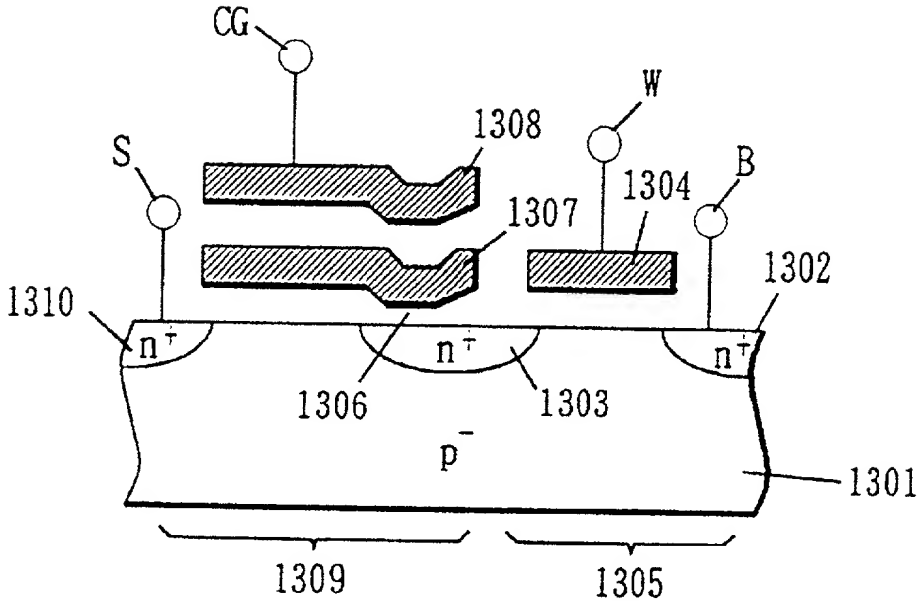


FIG. 144 PRIOR ART

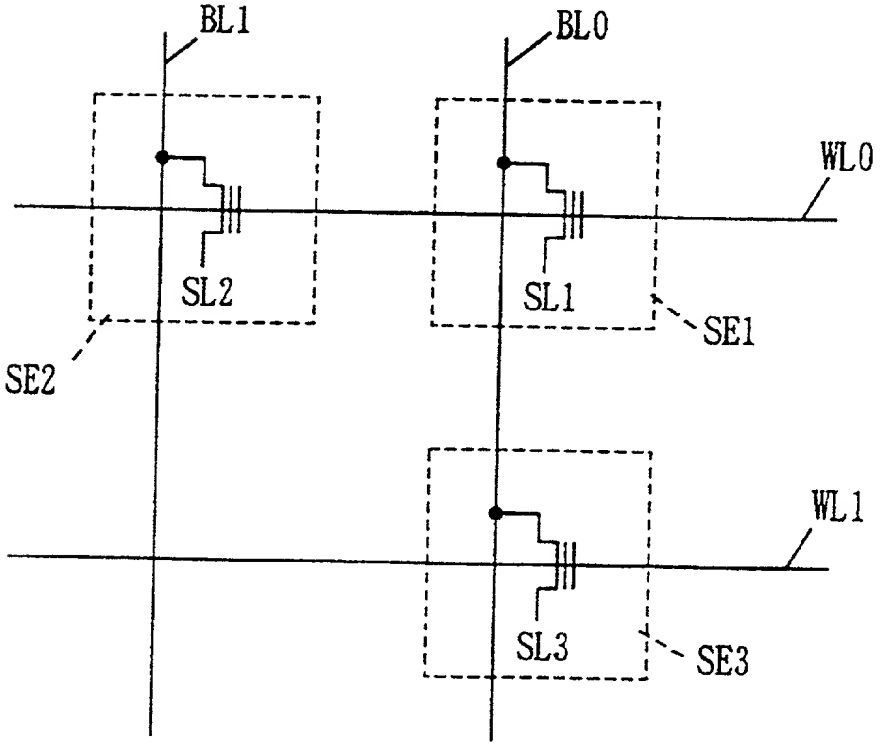
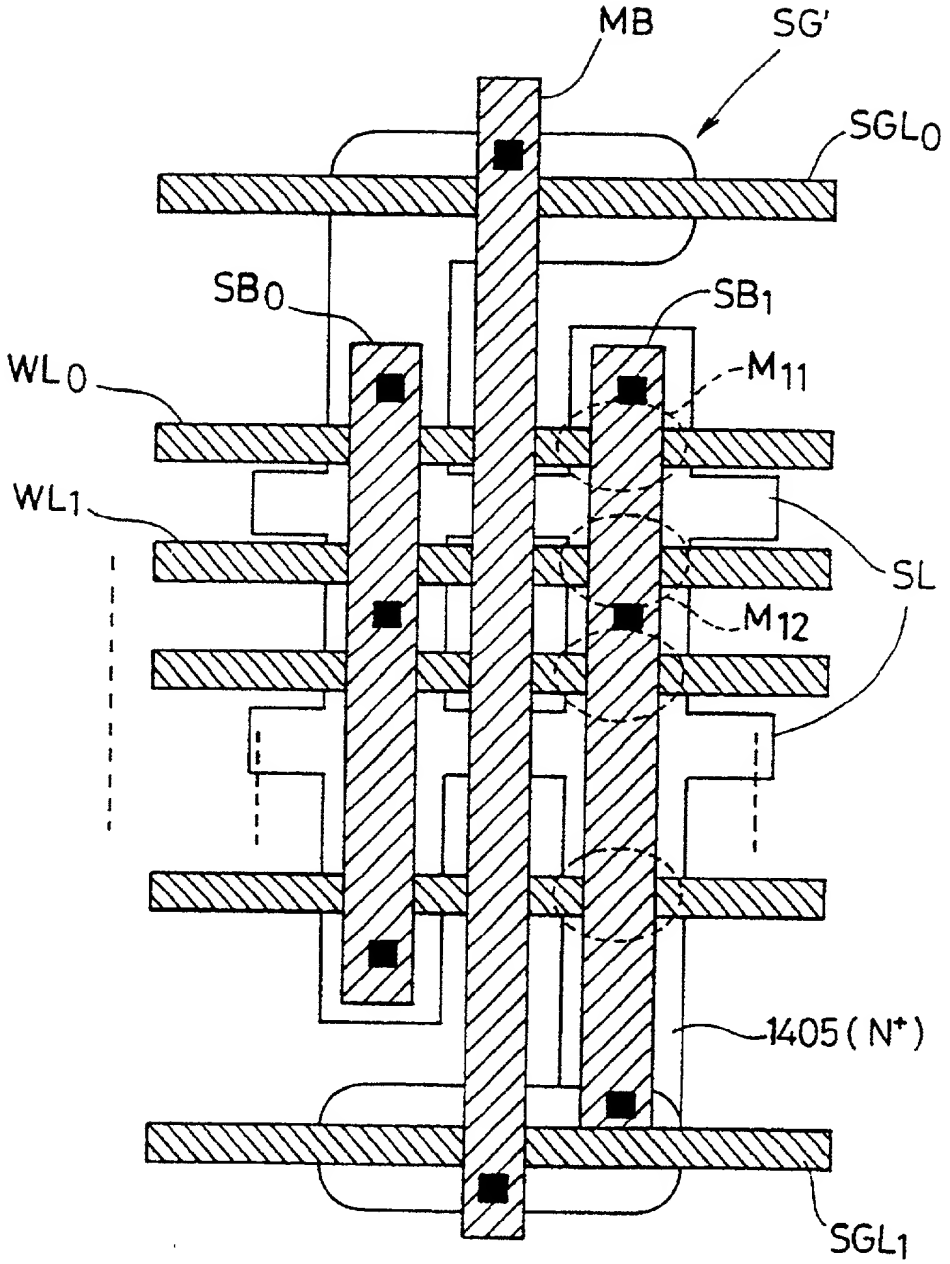


FIG. 145



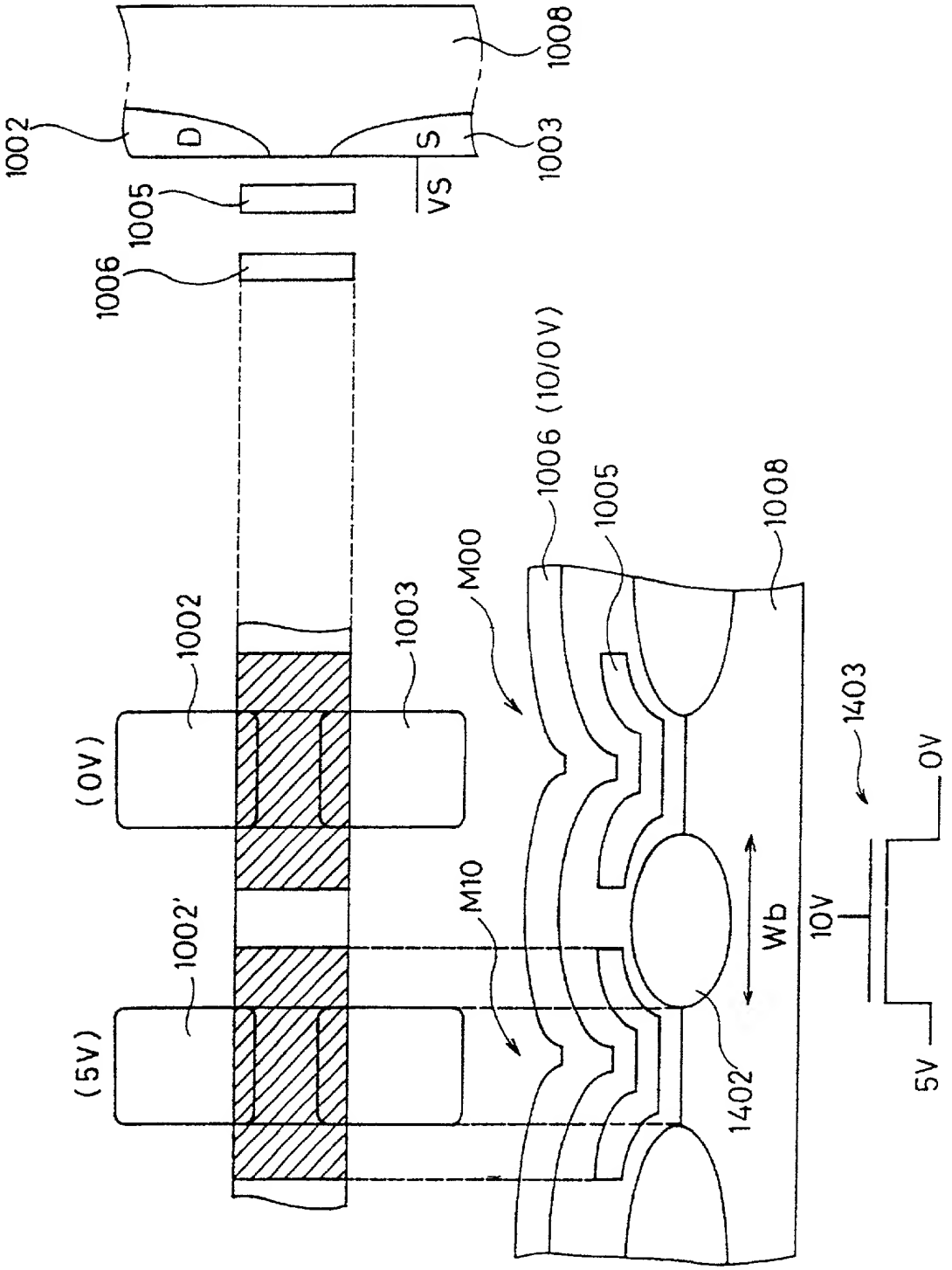

1002
D
S
1003
1008
VS
1005
1006
1006 (10/0V)
1005
1008
M00
1002
1003
(0V)
1403
0V
10V
Wb
1002'
M10
(5V)
1402
5V

FIG. 146

FIG. 147A

PROGRAM

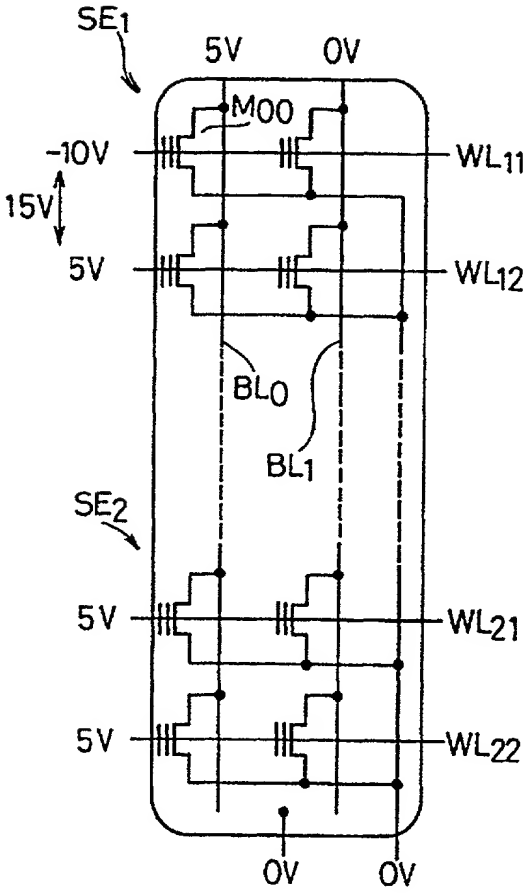
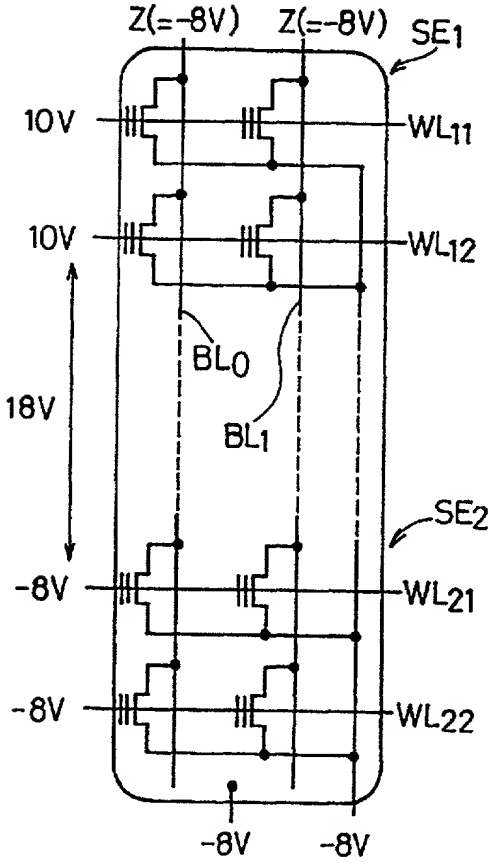


FIG. 147B

ERASE



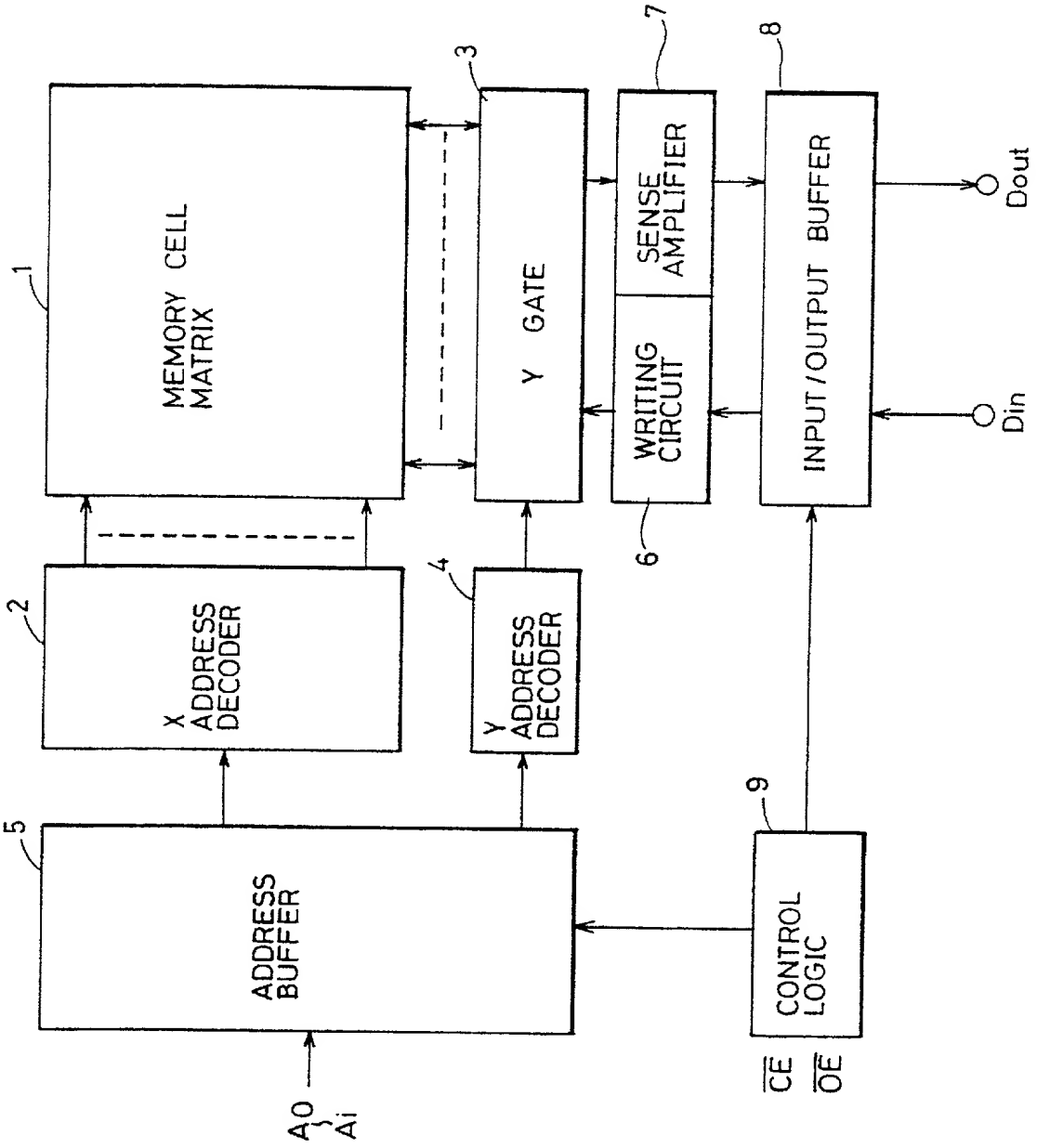

PRIOR ART
MEMORY CELL MATRIX
1
X ADDRESS DECODER
2
Y GATE
3
Y ADDRESS DECODER
4
ADDRESS BUFFER
5
WRITING CIRCUIT
6
SENSE AMPLIFIER
7
INPUT/OUTPUT BUFFER
8
CONTROL LOGIC
9
Dout
Din
A0
Ai
CE
OE

FIG. 148

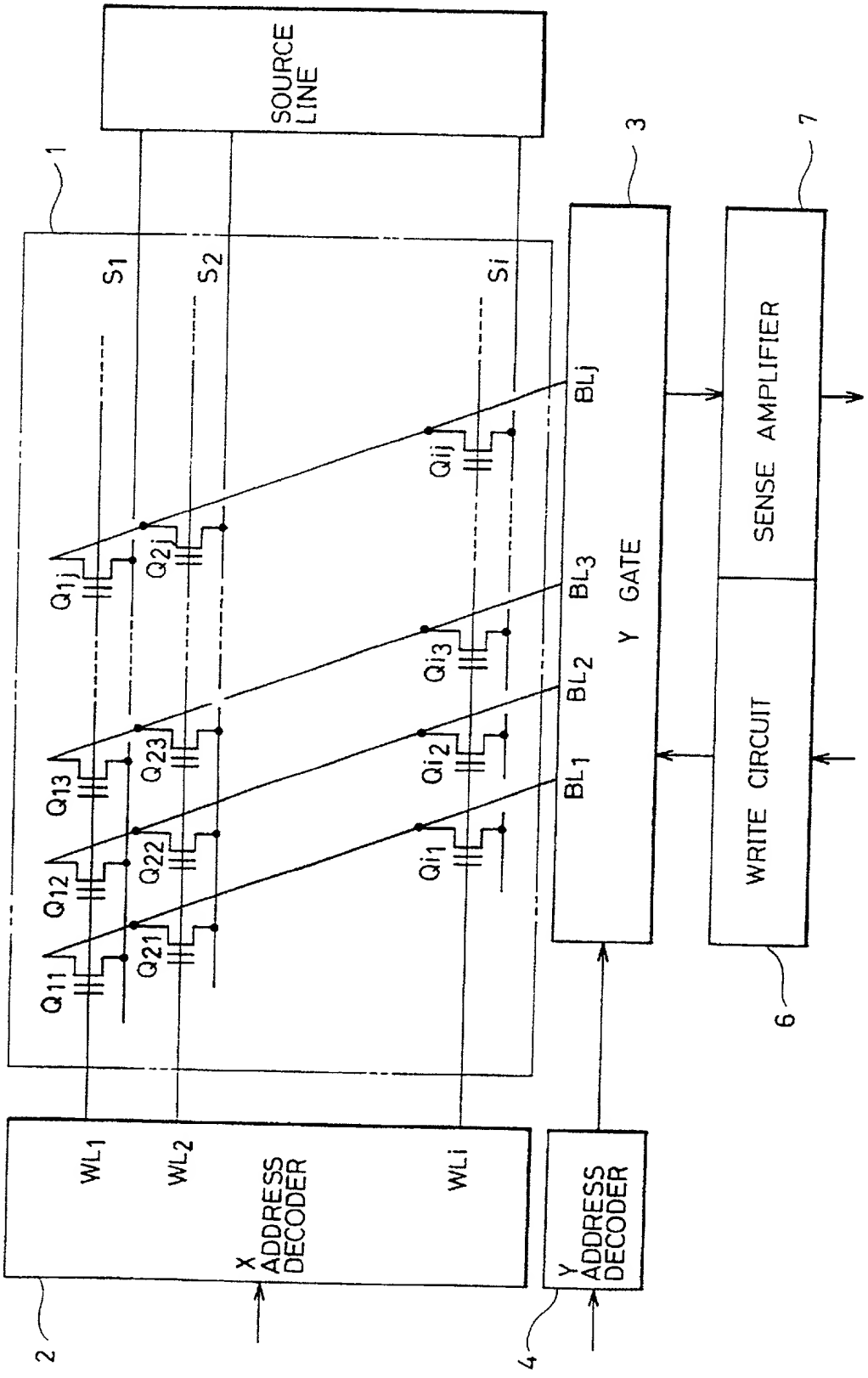


FIG. 149 PRIOR ART

FIG. 150 PRIOR ART

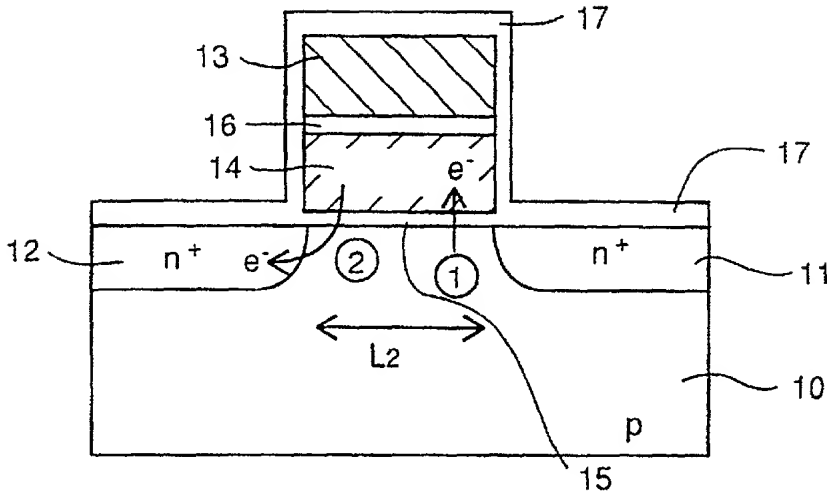


FIG. 151 PRIOR ART

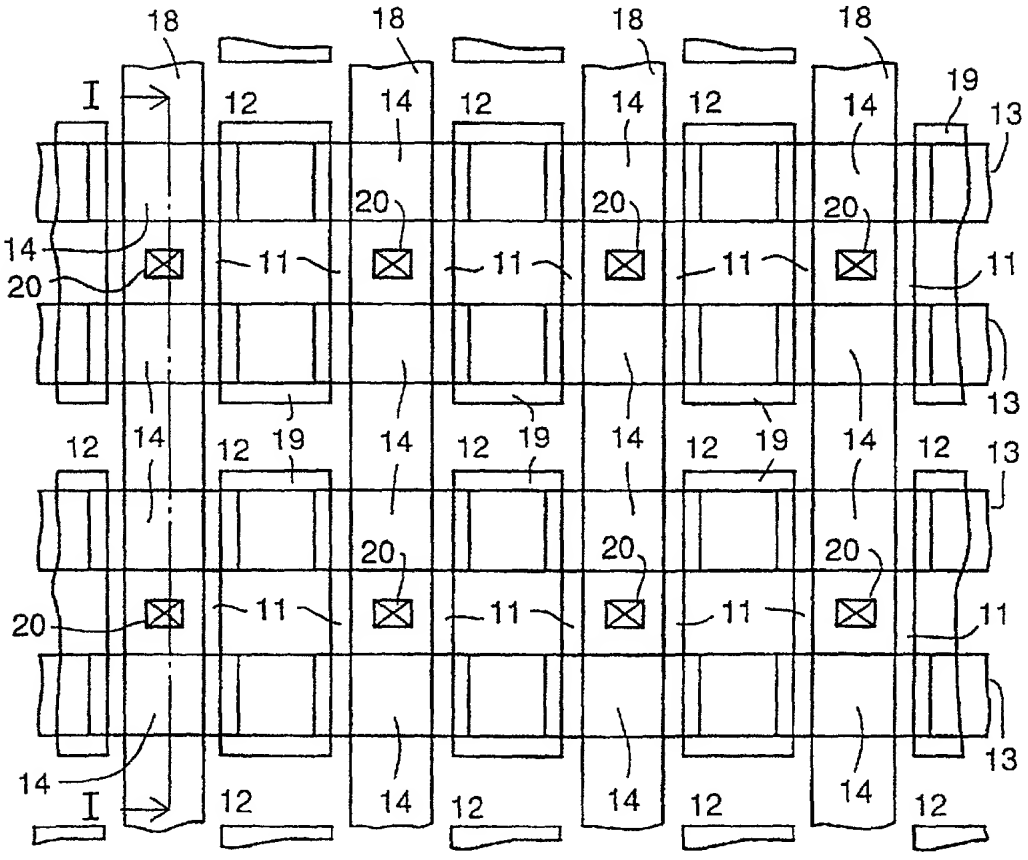


FIG. 152 PRIOR ART

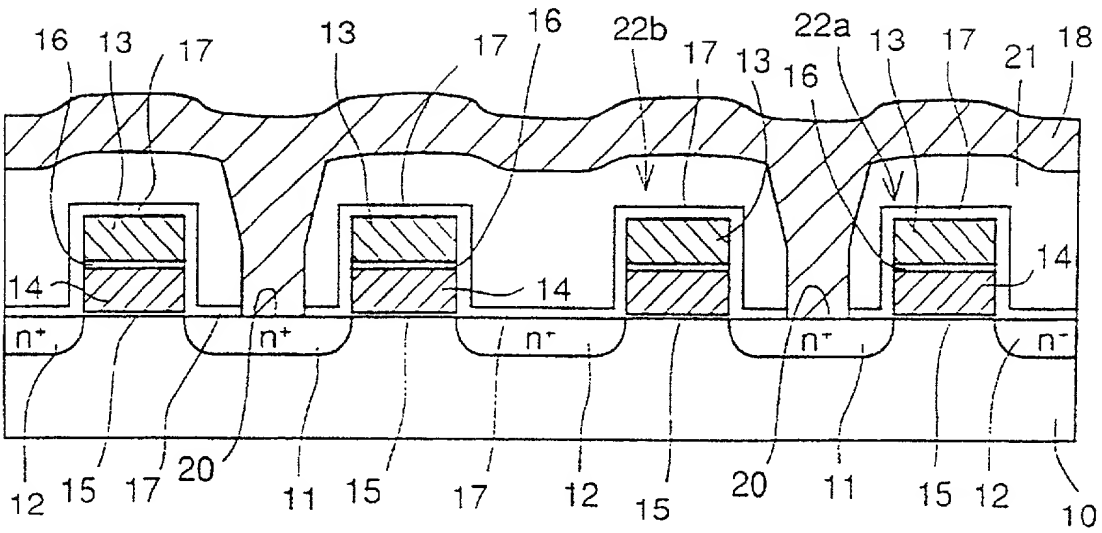


FIG. 153 PRIOR ART

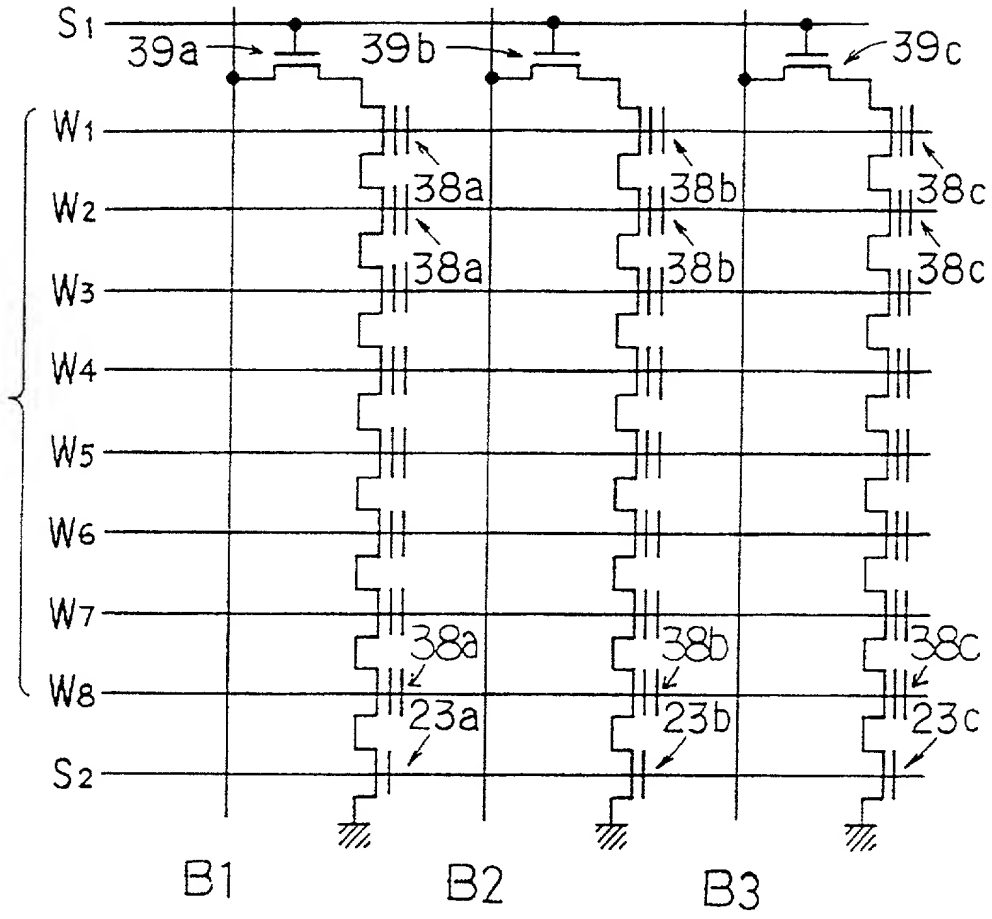


FIG. 154 PRIOR ART

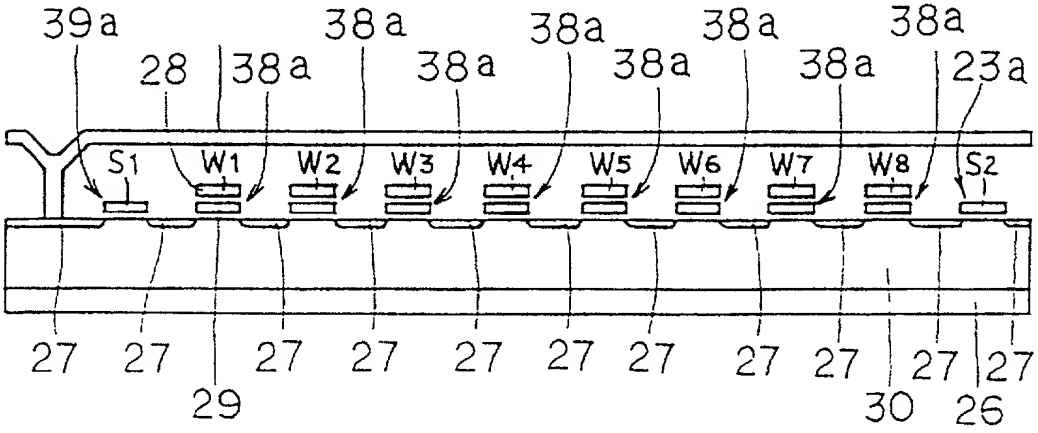


FIG. 155 PRIOR ART

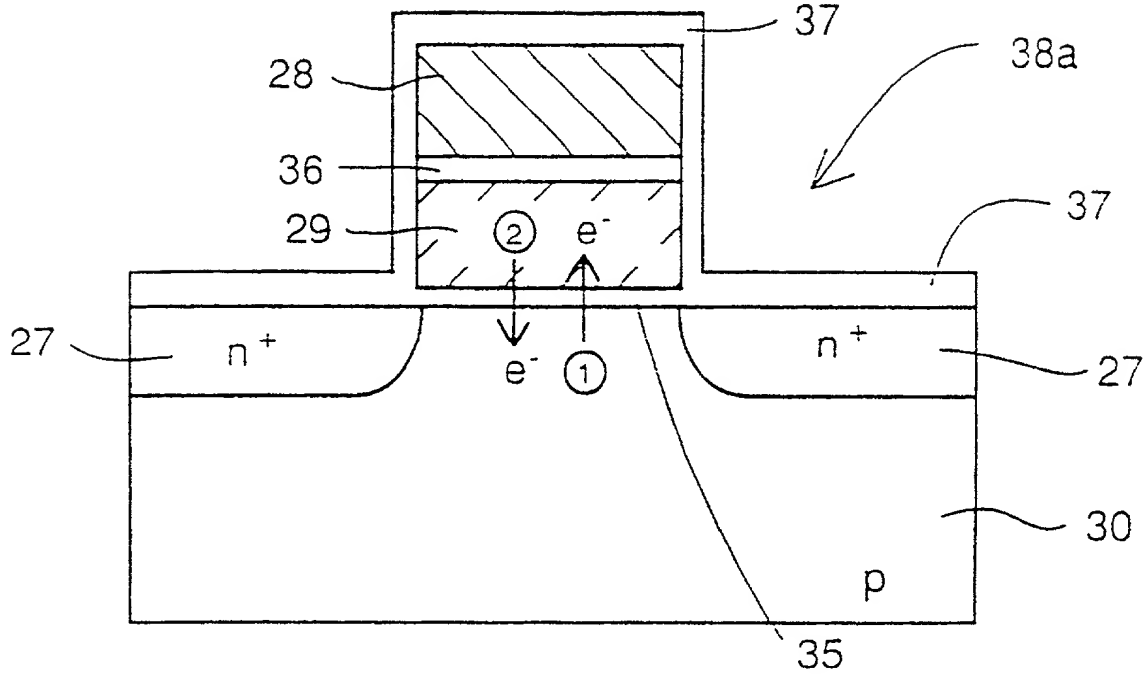


FIG. 156A PRIOR ART

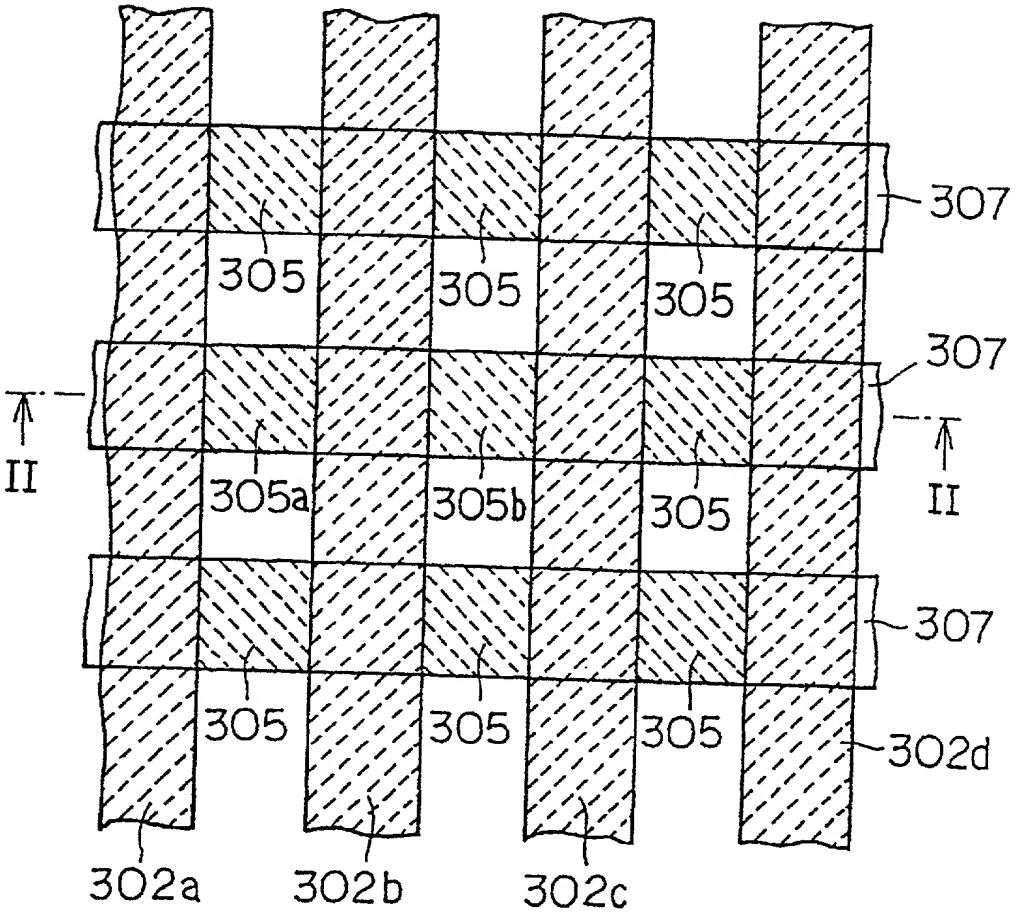


FIG. 156B PRIOR ART

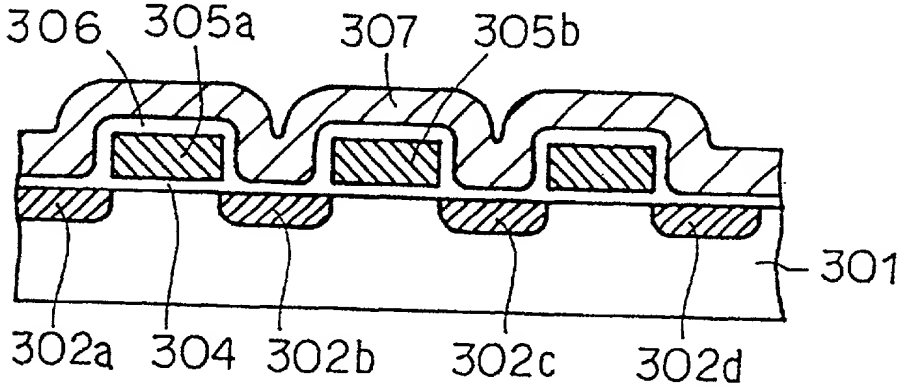


FIG. 157 PRIOR ART

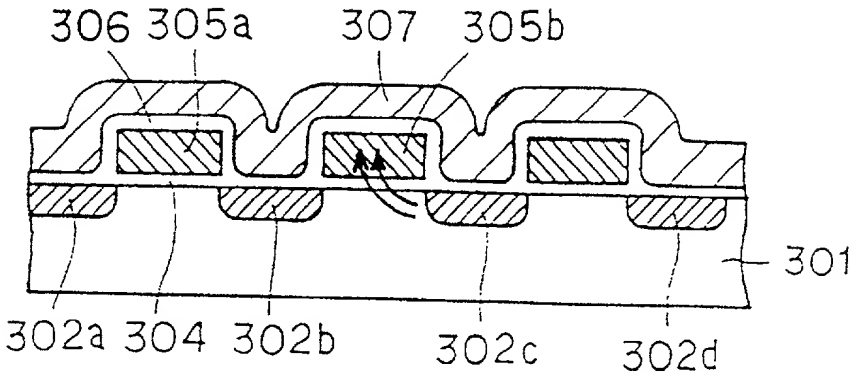


FIG. 158 PRIOR ART

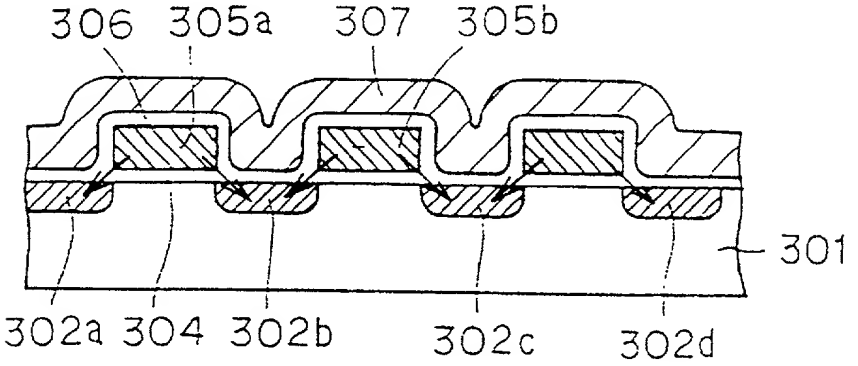


FIG. 159 PRIOR ART